

## BCM4375

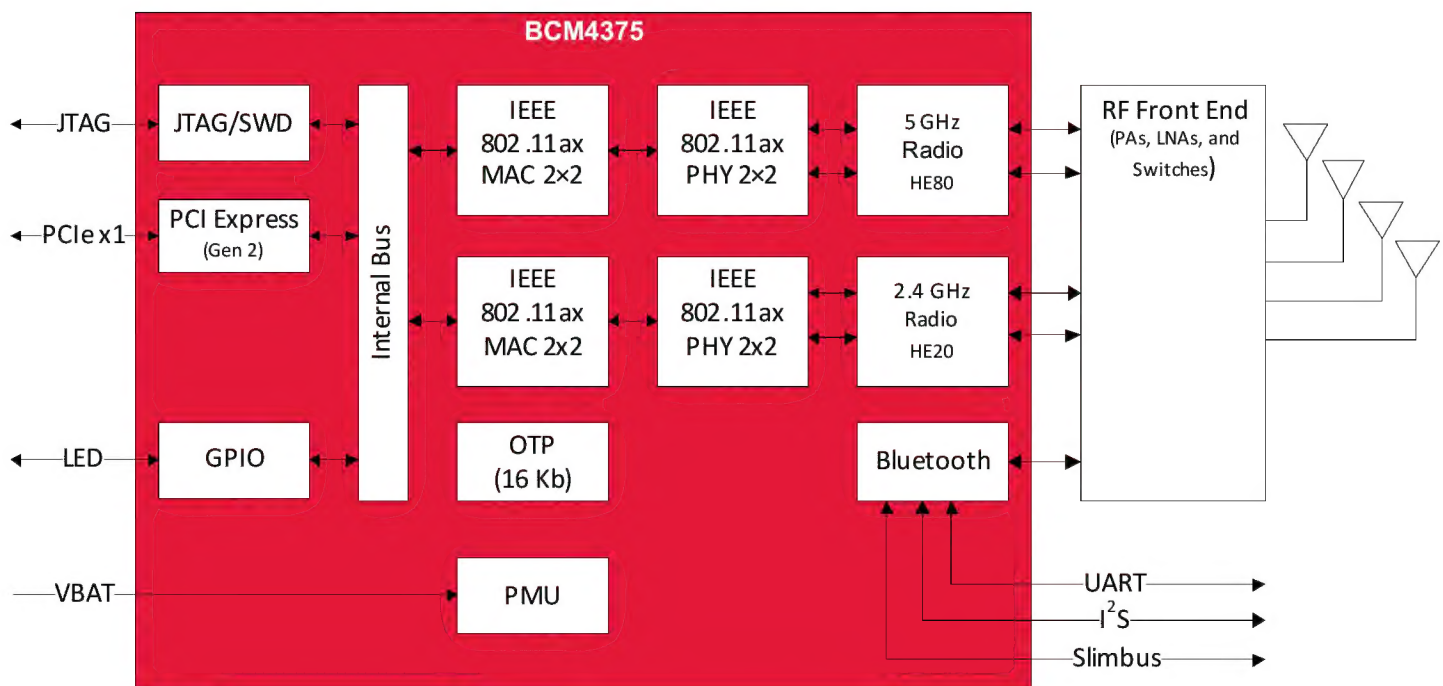
### Single-Chip 5G WiFi IEEE 802.11ax 2x2 MAC/Baseband/Radio with Integrated Bluetooth 5.0

#### General Description

The Broadcom® BCM4375 is a dual-band (2.4 GHz and 5 GHz) 2x2 IEEE 802.11ax draft-compliant and Bluetooth (BT) 5.0 system-on-a-chip.

The WLAN host interface is PCIe v3.0 compliant and runs at Gen2 speeds. The BT host interface is a high-speed 4-wire UART.

**Figure 1: BCM4375 Functional Block Diagram**



## Features

### IEEE 802.11 Key Features

- IEEE 802.11ax draft compliant.
- Data rate of up to 1200 Mbps during single-band operation and 1430 Mbps in RSDB mode.
- 20/40/80 MHz channels for the main (Main) 2x2 WLAN core (1024-QAM modulation), and 20 MHz channels for the auxiliary (Aux) 2x2 WLAN core (256-QAM modulation).
- Full IEEE 802.11a/b/g/n/ac legacy compatibility with enhanced performance.
- Zero wait dynamic frequency selection (DFS): background channel availability check (CAC) scan for immediate switch to candidate DFS channel.
- PCIe mode complies with PCI Express base specification revision 3.0 for x1 lane and power management running at Gen2 speeds.
- Integrated ARM Cortex R4 processor. On-chip memory includes 1600 KB SRAM and 1216 KB ROM.

## Features

### Bluetooth Key Features

- Complies with BT Core Specification Version 5.0 with support for future specifications.
- Interface support: host controller interface (HCI) using a high-speed UART interface and PCM for audio data.
- Supports serial flash interfaces.

### General Features

- Supports battery range from 3.0V to 5.25V.
- Supports 1406 bytes of user-accessible OTP, of which 512 bytes are allocated for BT and 894 bytes are allocated for WLAN for storing board parameters.
- GPIOs: 21
- Package: 651-bump WLCSP (6.225 mm × 6.130 mm, 0.2 mm pitch)

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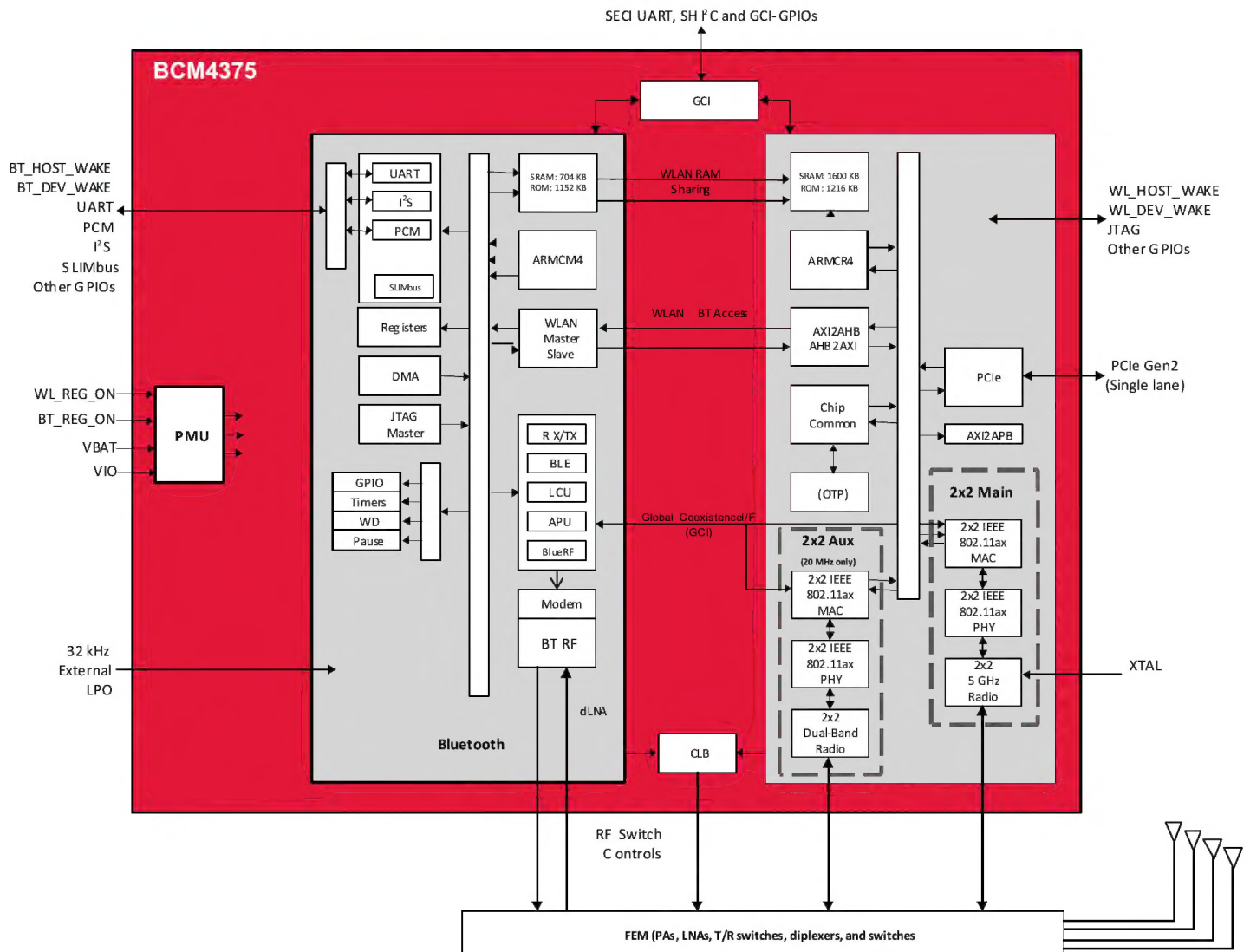
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# Chapter 1: Overview

The Broadcom® BCM4375 single-chip device includes an integrated IEEE 802.11 a/b/g/n/ac/ax MAC/baseband/radio (dual-core 2x2 MU-MIMO). It also supports Bluetooth 5.0 and Bluetooth Low Energy (BLE).

Figure 2 shows the interconnect of all the major physical blocks in the BCM4375 and their associated external interfaces, which are described in greater detail in the following sections.

**Figure 2: BCM4375 System Block Diagram**



## Chapter 2: DC Characteristics

**NOTE:** Values in this data sheet are design goals and are subject to change based on the results of device characterization.

### 2.1 Absolute Maximum Ratings

**CAUTION!** The absolute maximum ratings in [Table 1](#) indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

**Table 1: Absolute Maximum Ratings**

Rating	Symbol	Value	Unit
DC supply for VBAT	VBAT	−0.5 to +5.25	V
DC supply voltage for digital I/O	VDDIO	−0.5 to 2.07	V
DC supply voltage for RF switch I/Os	VDDIO_RF	−0.5 to 3.795	V
DC input supply voltage for MISCLDO	—	−0.5 to 1.28	V
DC supply voltage for RF analog	—	−0.5 to 1.15	V
DC supply voltage for core	—	−0.5 to 1.035	V
External TSSI Input	TSSI	−0.5 to 1.15	V
Maximum undershoot voltage for I/O <sup>a</sup>	V <sub>undershoot</sub>	−0.5	V
Maximum overshoot voltage for I/O <sup>a</sup>	V <sub>overshoot</sub>	VDDIO + 0.5	V
Maximum junction temperature	T <sub>j</sub>	125	°C

a. Duration not to exceed 25% of the duty cycle.

### 2.2 Environmental Ratings

The environmental ratings are shown in [Table 2](#).

**Table 2: Environmental Ratings**

Characteristic	Value	Units	Conditions/Comments
Ambient Temperature (T <sub>A</sub> )	−30 to +85	°C	Functional operation <sup>a</sup>
Storage Temperature	−40 to +125	°C	—
Relative Humidity	Less than 60	%	Storage
	Less than 85	%	Operation

a. Functionality is guaranteed across this range of temperature. Optimal RF performance specified in the data sheet, however, is guaranteed only for −10°C to +55°C without derating performance.

## 2.3 Recommended Operating Conditions and DC Characteristics

**CAUTION!** Functional operation is not guaranteed outside of the limits shown in Table 3, and operation outside these limits for extended periods can adversely affect long-term reliability of the device.

**Table 3: Recommended Operating Conditions and DC Characteristics**

Parameter	Symbol	Value			Unit
		Minimum	Typical	Maximum	
DC supply voltage for VBAT	VBAT	3.0 <sup>a</sup>	—	5.25	V
DC supply voltage for core	VDD	0.85	0.9	0.95	V
DC supply voltage for RF blocks in chip	VDDRF	0.95	1.0	1.05	V
DC supply voltage for digital I/O	VDDIO	1.62	1.8	1.98	V
DC supply voltage for analog I/O	VDDIOA, VDDIOP	1.62	1.8	1.98	V
DC supply voltage for RF switch I/Os when supporting 3.3V RF_SW_CTRL pads	VDDIO_RF <sup>b</sup>	3.13	3.3	3.46	V
DC supply voltage for RF switch I/Os when supporting 1.8V RF_SW_CTRL pads		1.62	1.8	1.98	V
External TSSI input	TSSI	0.15	—	0.95	V
Internal POR threshold	Vth_POR	0.4	—	0.7	V
<b>Other Digital I/O Pins</b>					
For VDDIO = 1.8V:					
Input high voltage	VIH	0.65 x VDDIO	—	—	V
Input low voltage	VIL	—	—	0.4 x VDDIO	V
Output high voltage @ 2 mA	VOH	VDDIO – 0.40	—	—	V
Output low voltage @ 2 mA	VOL	—	—	0.40	V
<b>RF Switch Control Output Pins<sup>c</sup></b>					
For VDDIO_RF = 1.8V:					
Output high voltage @ 2 mA	VOH	VDDIO_RF – 0.40	—	—	V
Output low voltage @ 2 mA	VOL	—	—	0.40	V
For VDDIO_RF = 3.3V:					
Output high voltage @ 2 mA	VOH	VDDIO_RF – 0.40	—	—	V
Output low voltage @ 2 mA	VOL	—	—	0.40	V
Input capacitance	C <sub>IN</sub>	—	—	5	pF

- The BCM4375 is functional across this range of voltages. Optimal RF performance specified in the data sheet, however, is guaranteed only for 3.2V < VBAT < 4.8V.
- The BCM4375 supports either 1.8V or 3.3V RF switch control pads. To select 1.8V, connect MODEHV and MODEHV1 to ground. To select 3.3V, connect MODEHV and MODEHV1 to 3.3V.
- Programmable 2 mA to 16 mA drive strength. Default is 10 mA.

## 2.4 Electrostatic Discharge Specifications

Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage. Proper use of wrist and heel grounding straps to discharge static electricity is required when handling these devices. Always store unused material in its antistatic packaging.

**Table 4: ESD Specifications**

Pin Type	Symbol	Condition	ESD Rating	Unit
ESD, Handling Reference: NQY00083, Section 3.4, Group D9, Table B	ESD_HAND_HBM	Human body model contact discharge per JEDEC EID/JESD22-A114	2000	V
CDM	ESD_HAND_CDM	Charged device model contact discharge per JEDEC EIA/JESD22- C101	350 <sup>a</sup>	V

a. 250V for O\_PAD\_BT\_13DBMOP.

# Chapter 3: Power Supplies and Power Management

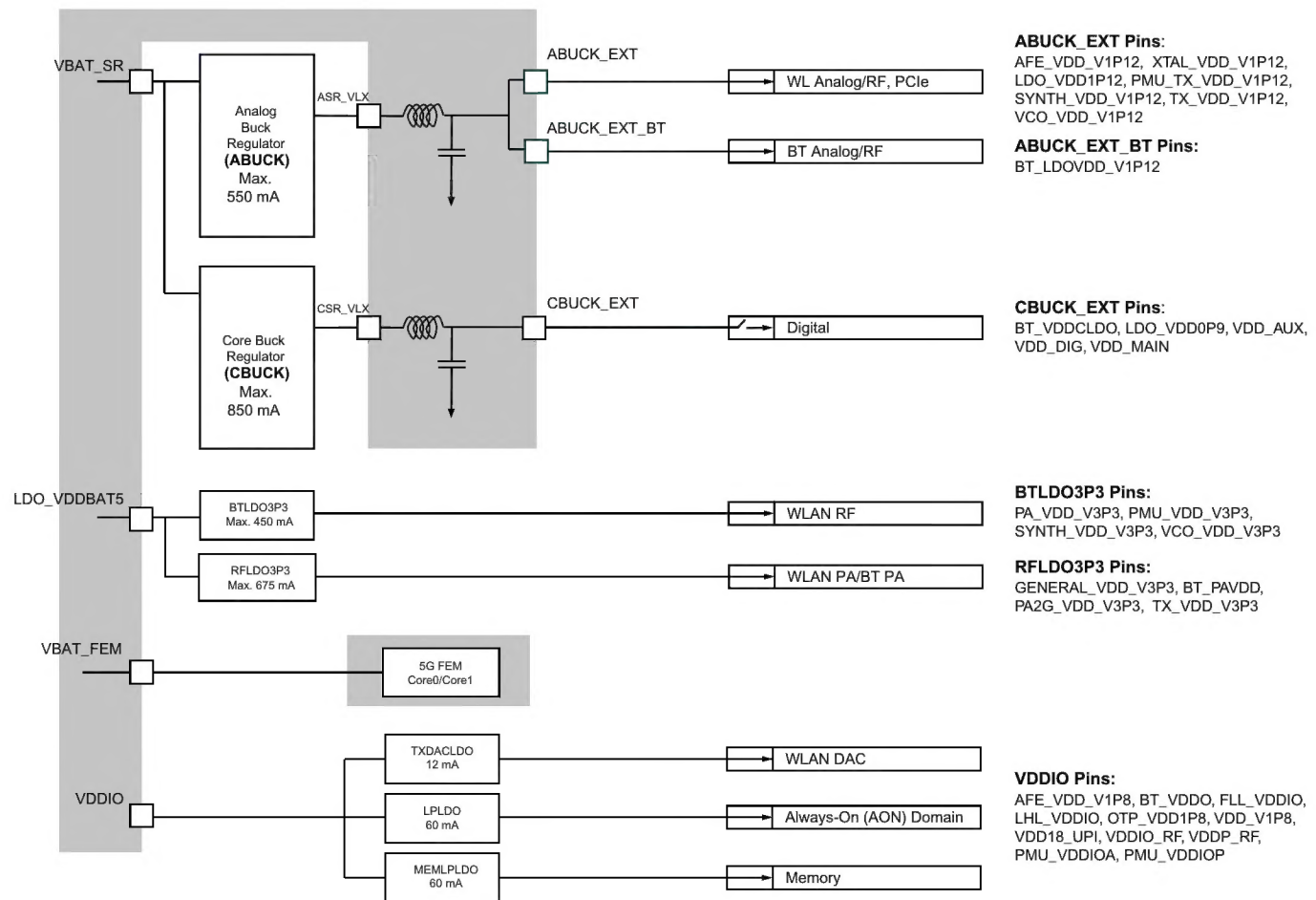
## 3.1 Power Supply Topology

The BCM4375 contains a power management unit (PMU) that is powered by VBAT (3.0V to 5.25V) and VDDIO (1.62V to 1.8V). All other voltages are provided by internal BCM4375 regulators.

Two control signals, BT\_REG\_ON and WL\_REG\_ON, are used to power-up the regulators and take the respective sections out of reset. All regulators are powered down only when both control signals are deasserted.

Figure 3 shows the typical BCM4375 power topology. The gray areas are external to the BCM4375.

Figure 3: Typical Power Topology



## 3.2 Power-Up/Power-Down/Reset Circuits

The host controls device power consumption via two signals, BT\_REG\_ON and WL\_REG\_ON. The state of BT\_REG\_ON determines whether Bluetooth subsystem circuits are enabled or disabled, and the state of WL\_REG\_ON determines whether WLAN subsystem circuits are enabled or disabled. If both signals are low, then internal regulators are disabled. For timing diagrams of these signals and the required power-up sequences, see [Section 6: “WLAN Global Functions and Interfaces,” on page 31](#).

[Table 5](#) provides the BT\_REG\_ON and WL\_REG\_ON electrical specification.

**Table 5: BT\_REG\_ON and WL\_REG\_ON Electrical Specification**

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input high voltage	$V_{IH}$	For WL_REG_ON	1	—	1.98	V
		For BT_REG_ON	1	—	1.98	V
Input low voltage	$V_{IL}$	—	VSS	—	0.3	V
Pull-down resistance	$R_{PD}$	Auto-enabled for input low; disabled for input high	—	50	—	k $\Omega$
Leakage discharged current	$I_{LEAK\_DIS}$	—	—	28	—	nA
REG OFF time	$T_{REG\_OFF}$	$C_{REG\_ON} \leq 10$ pF	2	—	—	ms
Reset hold time	—	Hold low to reset.	10	—	—	ms

## 3.3 Device Power Management

In addition to the BT\_REG\_ON and WL\_REG\_ON signals described in [“Power-Up/Power-Down/Reset Circuits” on page 10](#), the BCM4375 includes a PMU sequencer, which saves significant power by putting the BCM4375 into low-power modes pertinent to the operating environment and activities being performed.

[Table 6](#) describes the power modes. VBAT and VDDIO are both on for the modes shown in the table.

**Table 6: Power Modes**

Power Mode	WL_REG_ON	BT_REG_ON	Description
Active	On	On	All blocks are powered up and fully functional.
Deep-Sleep (low power)	On	On	Most of the chip is powered off, including all main clocks. The 32.768 kHz LPO clock is available only to the PMU sequencer so that it can wake the chip and transition to Active mode. Logic states are saved in retention memory and are restored upon a wake-up event triggered by PMU timers or an external interrupt.
Power-Down (low power)	Off	Off	The BCM4375 is effectively powered off by shutting down all internal regulators. External logic brings the chip out of this mode. <b>NOTE:</b> BT and WLAN operate independently and one or both may be placed in power-down mode at a time.

During long periods of inactivity, the BT and WLAN cores enter low-power modes. The device may be forced into the Power-Down mode by deasserting both WL\_REG\_ON and BT\_REG\_ON.

## 3.4 Bluetooth Subsystem Power Management

The BCM4375 may be configured so that dedicated signals are used for power management handshaking between the BCM4375 and the host. The basic power saving functions supported by those handshaking signals include the standard Bluetooth defined power savings modes and standby modes of operation. [Table 7](#) describes the power-control handshake signals used with the UART interface.

**Table 7: Power Control Pin Description**

Signal	Mapped to Pin	Type	Description
BT_DEV_WAKE	408	I	Bluetooth device wake-up: Signal from the host to the BCM4375 indicating that the host requires attention. <ul style="list-style-type: none"> <li>■ Asserted: The Bluetooth device must wake-up or remain awake.</li> <li>■ Deasserted: The Bluetooth device may sleep when sleep criteria are met.</li> </ul> The polarity of this signal is software configurable and can be asserted high or low.
BT_HOST_WAKE	377	O	Host wake up. Signal from the BCM4375 to the host indicating that the BCM4375 requires attention. <ul style="list-style-type: none"> <li>■ Asserted: host device must wake-up or remain awake.</li> <li>■ Deasserted: host device may sleep when sleep criteria are met.</li> </ul> The polarity of this signal is software configurable and can be asserted high or low.
BT_CLK_REQ	411	O	The BCM4375 asserts BT_CLK_REQ when Bluetooth or WLAN wants the host to turn on the reference clock. The BT_CLK_REQ polarity is active-high.
<b>NOTE:</b> Pad function Control Register is set to 0 for these pins. See <a href="#">Section 2: "DC Characteristics,"</a> on page 6 for more details.			

See [Figure 9](#) for the Bluetooth startup signaling sequence.

## 3.5 Internal Regulator Electrical Specifications

### 3.5.1 PMU

Table 8 provides the PMU electrical specification.

**Table 8: PMU Electrical Specification**

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input supply voltage	V <sub>BAT</sub>	—	3.0	3.6	5.25	V
I/O supply voltage	V <sub>DDIO</sub>	—	1.62	1.80	1.98	V
Input supply voltages ramp-up time	T <sub>ramp</sub>	—	40 $\mu$ s	—	100 ms	—
Power up time	T <sub>PU</sub>	CSR output reaching 0.9V with respect to REG_ON	—	295	—	$\mu$ s
		ASR output reaching 1.12V with respect to REG_ON	—	315	—	$\mu$ s
V <sub>BAT</sub> UVLO threshold	V <sub>UVLO_rise</sub>	Rising	—	2.43	—	V
	V <sub>UVLO_fall</sub>	Falling	—	2.28	—	V
V <sub>DDIO</sub> brownout threshold	V <sub>BRWO_rise</sub>	Rising	—	1.597	—	V
	V <sub>BRWO_fall</sub>	Falling	—	1.424	—	V

Table 9 provides the electrical specification of the internal regulators.

**Table 9: Regulators Electrical Specification**

Regulator	Input Supply Voltage (V)			Output Current (mA)		
	Minimum	Typical	Maximum	Minimum	Typical	Maximum
ABUCK	3	3.6	5.25	—	—	550
CBUCK	3	3.6	5.25	—	—	850
RFLDO3P3	3	3.6	5.25	0.3	—	675
BTLDO3P3	3	3.6	5.25	0.2	—	450
LPLDO	1.62	1.8	1.98	0.001	—	60
MEMLPLDO	1.62	1.8	1.98	0.001	—	60
TXDACLDO	1.62	1.8	1.98	0.05	—	12

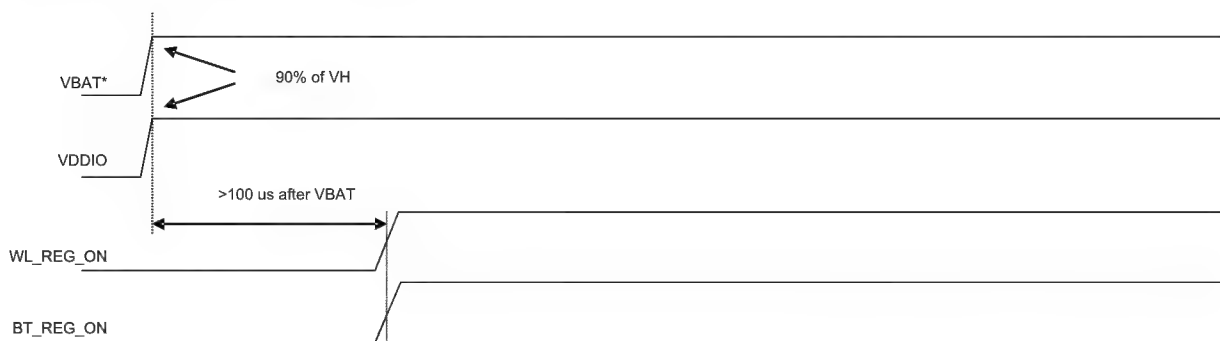
### 3.6 Reset and Startup Control Signal Sequencing

The BCM4375 has two signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described in [Table 5](#). Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states (see [Figure 4](#), [Figure 5](#), and [Figure 6](#) and [Figure 7](#)). The timing values indicated are minimum required values; longer delays are also acceptable.

**NOTE:** The BCM4375 has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after CBUCK\_EXT, ABUCK\_EXT, and VDDIO have passed the POR threshold. Wait at least 150 ms after CBUCK\_EXT, ABUCK\_EXT, and VDDIO are available before initiating PCIe accesses. See [Figure 3](#) for the CBUCK\_EXT and ABUCK\_EXT pins.

**NOTE:** The VBAT and VDDIO 10%–90% rise times should not be faster than 40  $\mu$ s.

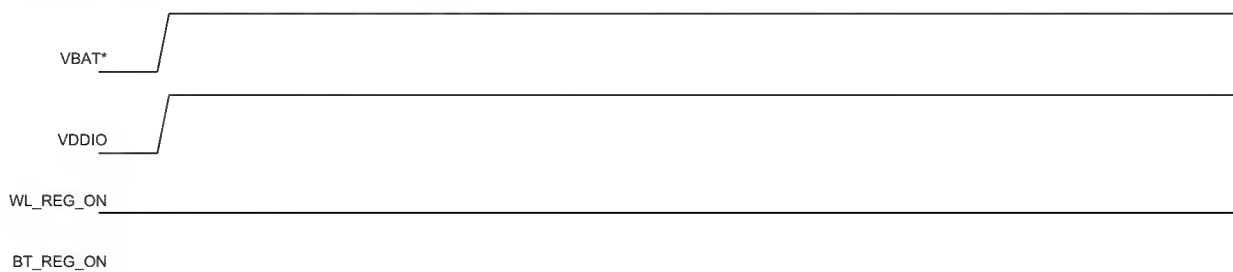
**Figure 4: WLAN = ON, Bluetooth = ON**



**\*Notes:**

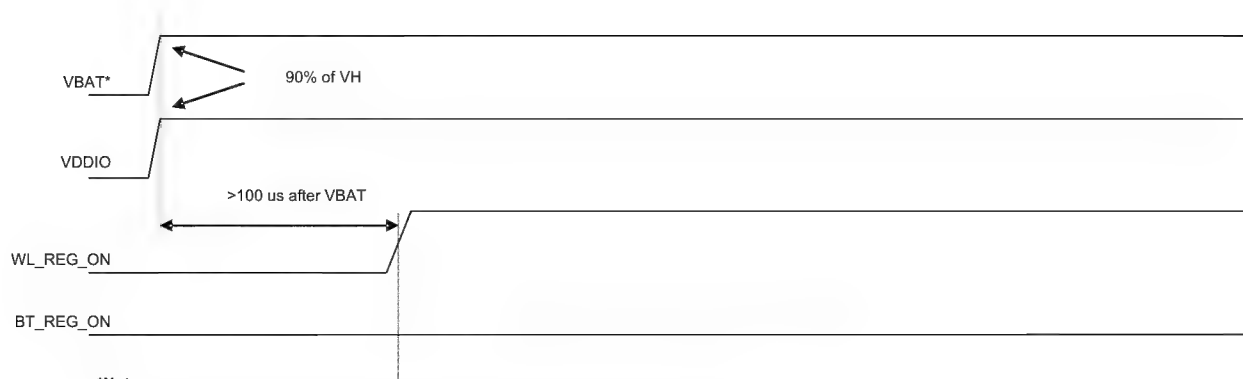
1. The VBAT and VDDIO 10%–90% rise times should be less than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

**Figure 5: WLAN = OFF, Bluetooth = OFF**

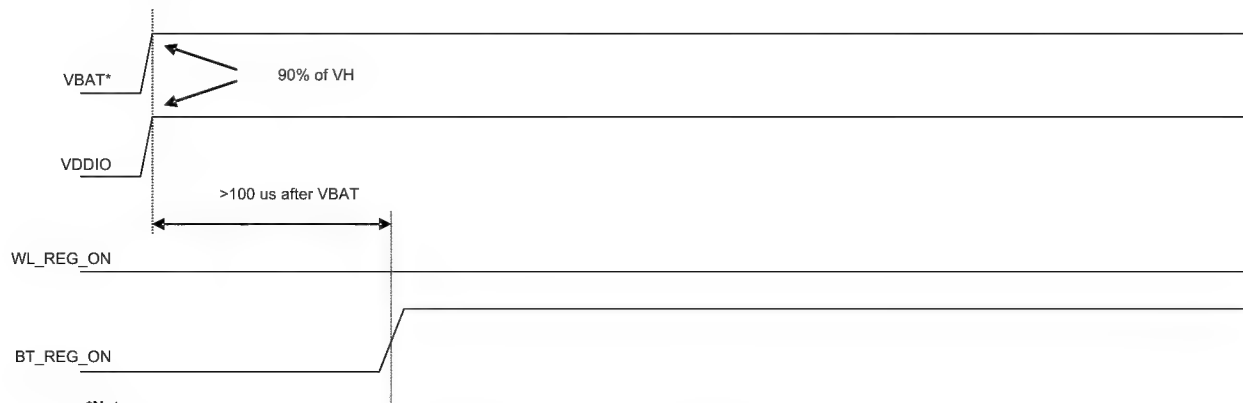


**\*Notes:**

1. The VBAT and VDDIO 10%–90% rise times should be less than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

**Figure 6: WLAN = ON, Bluetooth = OFF****\*Notes:**

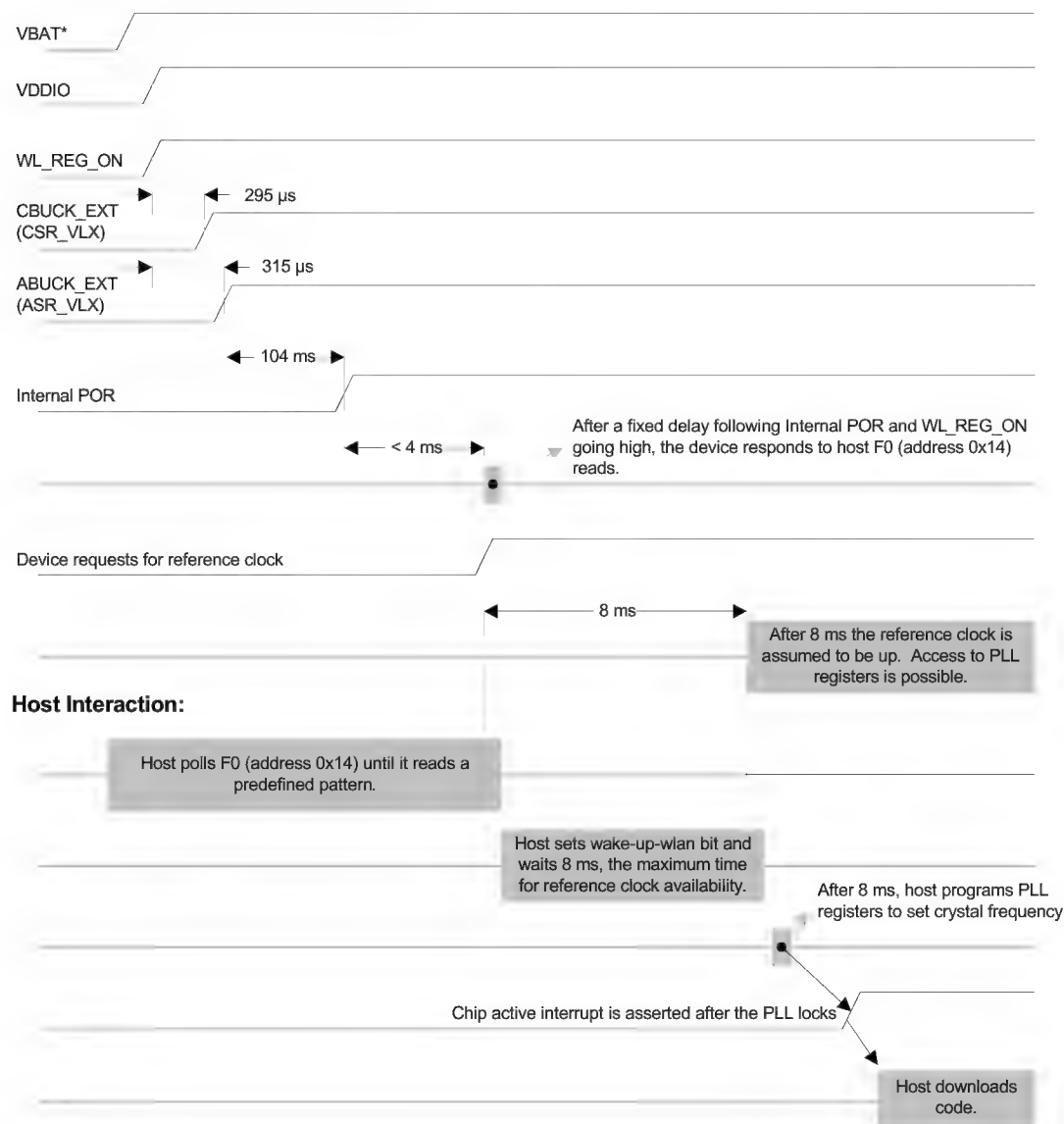
1. The VBAT and VDDIO 10%–90% rise times should be less than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

**Figure 7: WLAN = OFF, Bluetooth = ON****\*Notes:**

1. The VBAT and VDDIO 10%–90% rise times should be less than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

Figure 8 shows the WLAN boot-up sequence from power-up to firmware download.

**Figure 8: WLAN Boot-Up Sequence**

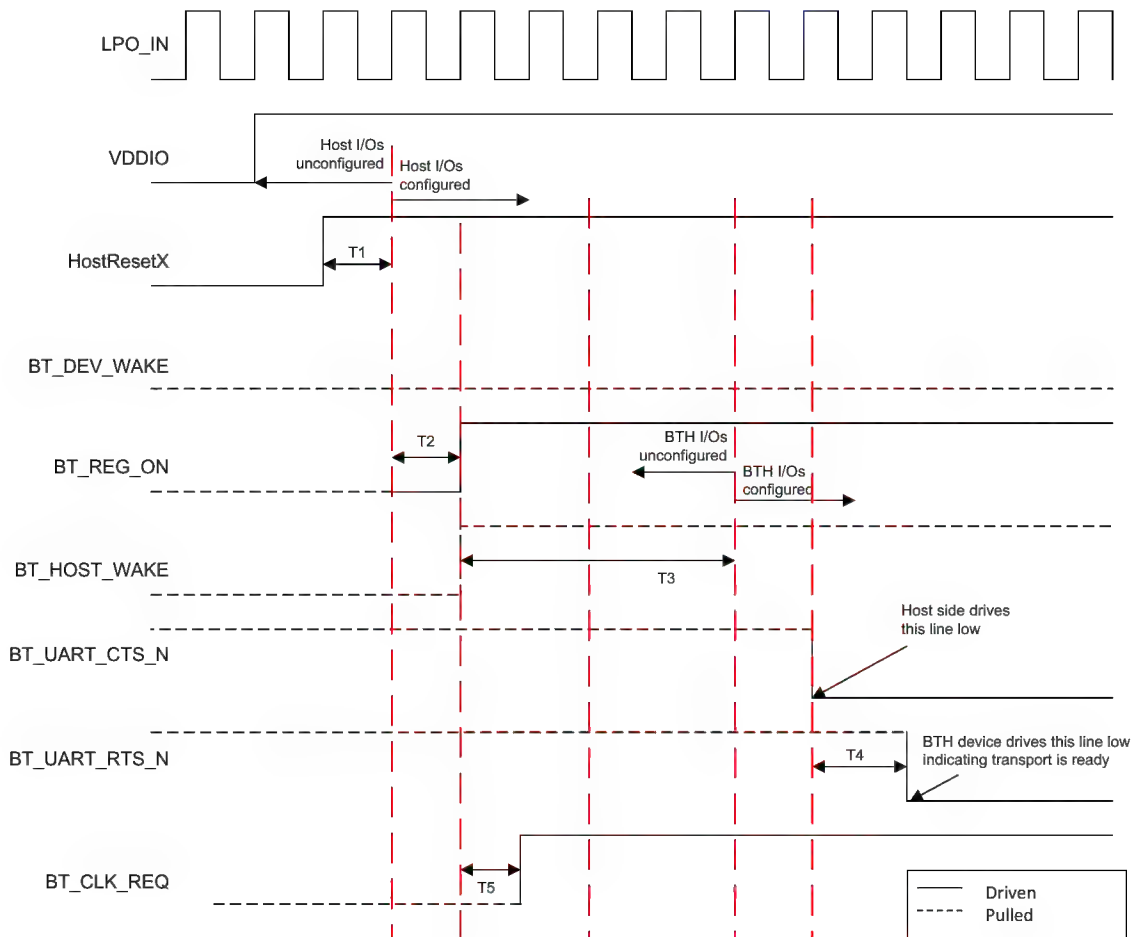


**\*Notes:**

1. The VBAT and VDDIO 10%–90% rise times should be less than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

The Bluetooth startup sequence timing is defined in [Figure 9](#).

**Figure 9: Bluetooth Subsystem Startup Signaling Sequence**



**Notes:**

- T1 is the time for Host to settle its I/Os after a reset.
- T2 is the time for Host to drive BT\_REG\_ON high after the Host I/Os are configured.
- T3 is the time for BTH (Bluetooth) device to settle its I/Os after a reset and reference clock settling time has elapsed.
- T4 is the time for BTH device to drive BT\_UART\_RTS\_N low after the Host drives BT\_UART\_CTS\_N low. This assumes the BTH device has already completed initialization.
- T5 is the time for BTH device to drive CLK\_REQ\_OUT high after BT\_REG\_ON goes high. Note this pin is used for designs that use an external reference clock source from the Host. This pin is irrelevant for Crystal reference clock based designs where the BTH device generates its own reference clock from an external crystal connected to its oscillator circuit.
- Timing diagram assumes VBAT is present.

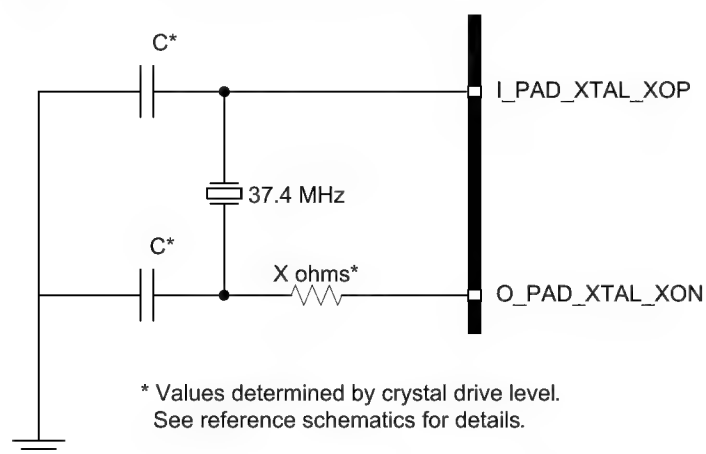
## Chapter 4: Frequency References

An external crystal is used for generating all radio frequencies and normal operation clocking. In addition, a low-power oscillator (LPO) is provided for lower power mode timing.

### 4.1 Crystal Interface and Clock Generation

The BCM4375 uses an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator including all external components is shown in [Figure 10](#). Consult the reference schematics for the latest configuration.

**Figure 10: Recommended Oscillator Configuration**



The frequency reference is a 37.4 MHz crystal. The signal characteristics for the crystal oscillator interface are provided in [Table 10](#).

**Table 10: Crystal Oscillator Requirements**

Parameter	Crystal <sup>a</sup>	Units
Frequency 2.4 GHz and 5 GHz bands: IEEE 802.11ax operation, PCIe WLAN interface	37.4	MHz
Frequency tolerance over the lifetime of the equipment, including temperature <sup>b</sup> , and without trimming.	±20	ppm
Crystal load capacitance	6–16	pF
ESR	< 60	Ω
Drive level (External crystal must be able to tolerate this drive level.)	> 200	μW

a. (Crystal) Use I\_PAD\_XTAL\_XOP and O\_PAD\_XTAL\_XON.

b. It is the responsibility of the equipment designer to select oscillator components that comply with these specifications.

## 4.2 External 32.768 kHz Low-Power Oscillator

The BCM4375 uses a secondary low-frequency clock for Low-Power mode timing. Either the internal low-precision LPO or an external 32.768 kHz precision oscillator is required. The internal LPO frequency range is approximately 33 kHz ( $\pm 30\%$ ) over process, voltage, and temperature, which is adequate for some applications. However, one trade-off caused by this wide LPO tolerance is a small current consumption increase during power save mode that is incurred by the need to wake up earlier to avoid missing beacons.

Whenever possible, the preferred approach is to use a precision external 32.768 kHz clock which meets the requirements listed in [Table 11](#).

**Table 11: External 32.768 kHz Sleep Clock Specifications**

Parameter	LPO Clock	Unit
Nominal input frequency	32.768	kHz
Frequency accuracy	$\pm 200$	ppm
Duty cycle	30–70	%
Input signal amplitude	200–3300	mV, p-p
Signal type	Square-wave or sine-wave	–
Input impedance <sup>a</sup>	> 100k	$\Omega$
	< 5	pF

a. When power is applied or switched off.

## Chapter 5: Bluetooth Subsystem

### 5.1 Overview

The Broadcom BCM4375 is a Bluetooth 5.0 + EDR-compliant, baseband processor/2.4 GHz transceiver, which presents a standard Host Controller Interface (HCI) via a high-speed UART and PCM for audio. The Bluetooth microprocessor core is based on the ARM Cortex-M4 32-bit RISC processor with embedded ICE-RT debug and JTAG interface units. The ARM core is paired with a memory unit that contains 1152 KB of ROM memory for program storage and boot ROM, and 704 KB of RAM for data scratch-pad and patch RAM code. At power-up, the lower-layer protocol stack is executed from the internal ROM memory. External patches may be applied to the ROM-based firmware to provide flexibility for bug fixes or features additions. These patches may be downloaded from the host to the BCM4375 through the UART transports.

### 5.2 PCM Interface

The BCM4375 supports two independent PCM interfaces that share the pins with the I<sup>2</sup>S interfaces. The PCM Interface on the BCM4375 can connect to linear PCM codec devices in master or slave mode. In master mode, the BCM4375 generates the BT\_PCM\_CLK and BT\_PCM\_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the BCM4375.

The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

#### 5.2.1 Slot Mapping

The BCM4375 supports up to three simultaneous full-duplex SCO or eSCO channels through the PCM interface. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8 kHz or 16 kHz audio sample interval is divided into as many as 16 slots. The number of slots is dependent on the selected interface rate of 128 kHz, 512 kHz, or 1024 kHz. The corresponding number of slots for these interface rate is 1, 2, 4, 8, and 16, respectively. Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

#### 5.2.2 Frame Synchronization

The BCM4375 supports both short- and long-frame synchronization in both master and slave modes. In short-frame synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is three bit periods and the pulse starts coincident with the first bit of the first slot.

#### 5.2.3 Data Formatting

The BCM4375 may be configured to generate and accept several different data formats. For conventional narrowband speech mode, the BCM4375 uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM interface. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sign bit, or a programmed value on the output. The default format is 13-bit 2's complement data, left justified, and clocked MSB first.

## 5.2.4 Wideband Speech Support

When the host encodes wideband speech (WBS) packets in transparent mode, the encoded packets are transferred over the PCM bus for an eSCO voice connection. In this mode, the PCM bus is typically configured in master mode for a 4 kHz sync rate with 16-bit samples, resulting in a 64 kbps bit rate. The BCM4375 also supports slave transparent mode using a proprietary rate-matching scheme. In SBC-code mode, linear 16-bit data at 16 kHz (256 kbps rate) is transferred over the PCM bus.

## 5.2.5 Burst PCM Mode

In this mode of operation, the PCM bus runs at a significantly higher rate of operation to allow the host to duty cycle its operation and save current. In this mode of operation, the PCM bus can operate at a rate of up to 24 MHz. This mode of operation is initiated with an HCI command from the host.

## 5.2.6 PCM Interface Timing

### 5.2.6.1 Short Frame Sync, Master Mode

Figure 11: PCM Timing Diagram (Short Frame Sync, Master Mode)

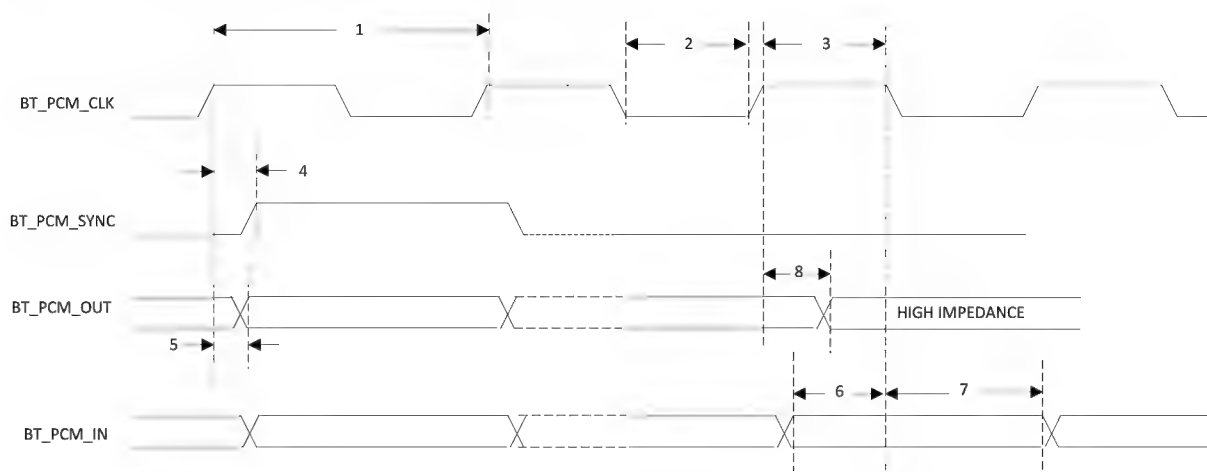


Table 12: PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	—	—	12	MHz
2	PCM bit clock low	41	—	—	ns
3	PCM bit clock high	41	—	—	ns
4	BT_PCM_SYNC delay	0	—	25	ns
5	BT_PCM_OUT delay	0	—	25	ns
6	BT_PCM_IN setup	8	—	—	ns
7	BT_PCM_IN hold	8	—	—	ns
8	Delay from rising edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high impedance.	0	—	25	ns

### 5.2.6.2 Short Frame Sync, Slave Mode

Figure 12: PCM Timing Diagram (Short Frame Sync, Slave Mode)

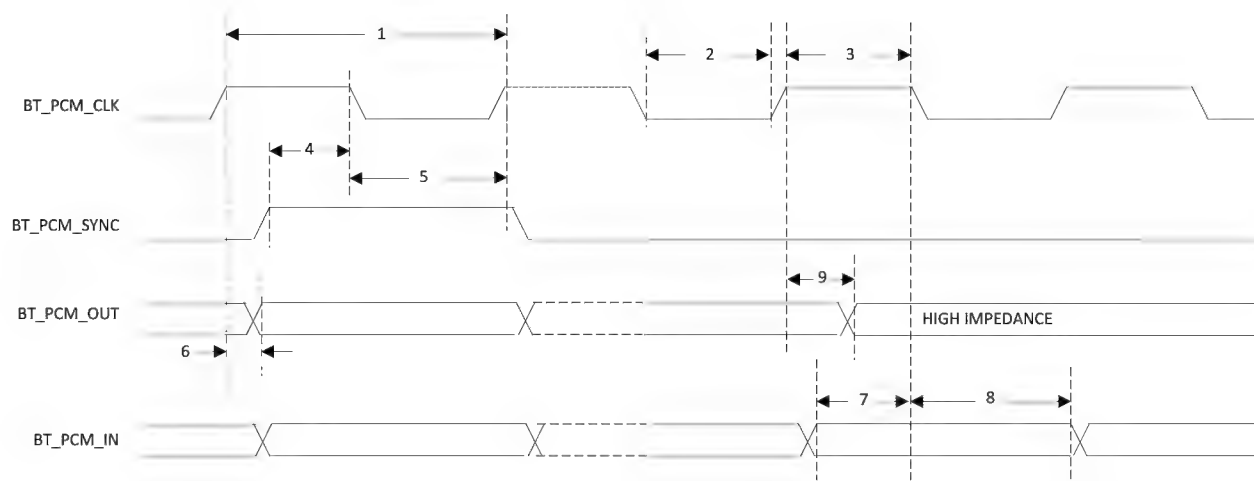


Table 13: PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	—	—	12	MHz
2	PCM bit clock low	41	—	—	ns
3	PCM bit clock high	41	—	—	ns
4	BT_PCM_SYNC setup	8	—	—	ns
5	BT_PCM_SYNC hold	8	—	—	ns
6	BT_PCM_OUT delay	0	—	25	ns
7	BT_PCM_IN setup	8	—	—	ns
8	BT_PCM_IN hold	8	—	—	ns
9	Delay from rising edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high impedance.	0	—	25	ns

5.2.6.3 Long Frame Sync, Master Mode

Figure 13: PCM Timing Diagram (Long Frame Sync, Master Mode)

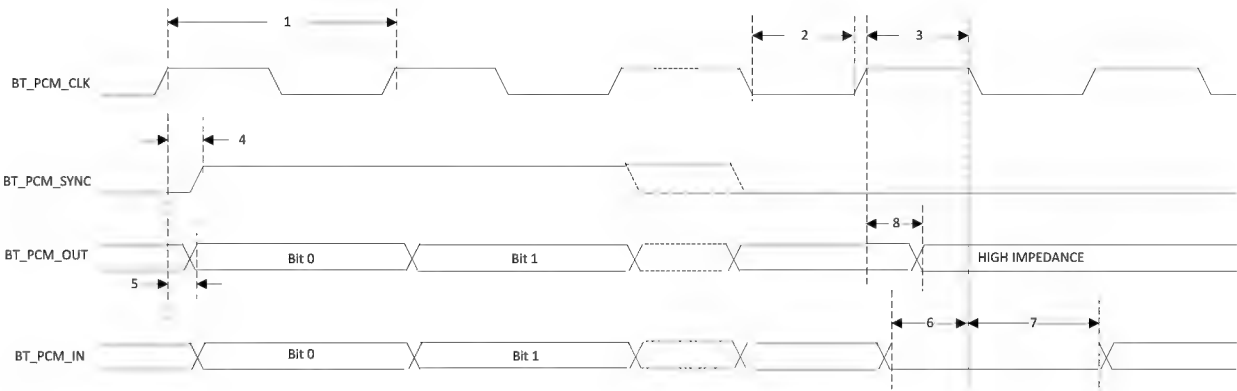


Table 14: PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	—	—	12	MHz
2	PCM bit clock low	41	—	—	ns
3	PCM bit clock high	41	—	—	ns
4	BT_PCM_SYNC delay	0	—	25	ns
5	BT_PCM_OUT delay	0	—	25	ns
6	BT_PCM_IN setup	8	—	—	ns
7	BT_PCM_IN hold	8	—	—	ns
8	Delay from rising edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high impedance.	0	—	25	ns

5.2.6.4 Long Frame Sync, Slave Mode

Figure 14: PCM Timing Diagram (Long Frame Sync, Slave Mode)

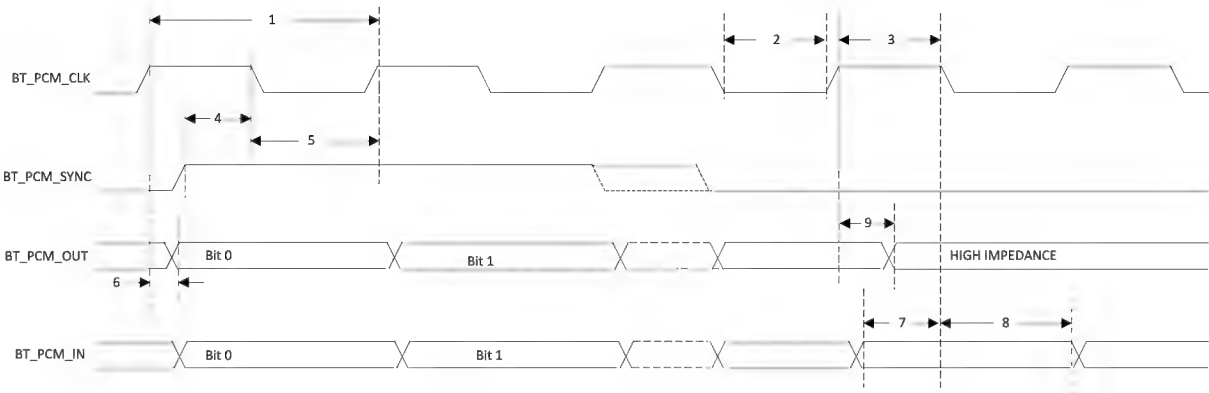


Table 15: PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	—	—	12	MHz
2	PCM bit clock low	41	—	—	ns
3	PCM bit clock high	41	—	—	ns
4	BT_PCM_SYNC setup	8	—	—	ns
5	BT_PCM_SYNC hold	8	—	—	ns
6	BT_PCM_OUT delay	0	—	25	ns
7	BT_PCM_IN setup	8	—	—	ns
8	BT_PCM_IN hold	8	—	—	ns
9	Delay from rising edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high impedance.	0	—	25	ns

5.2.6.5 Short Frame Sync, Burst Mode

Figure 15: PCM Burst Mode Timing (Receive Only, Short Frame Sync)

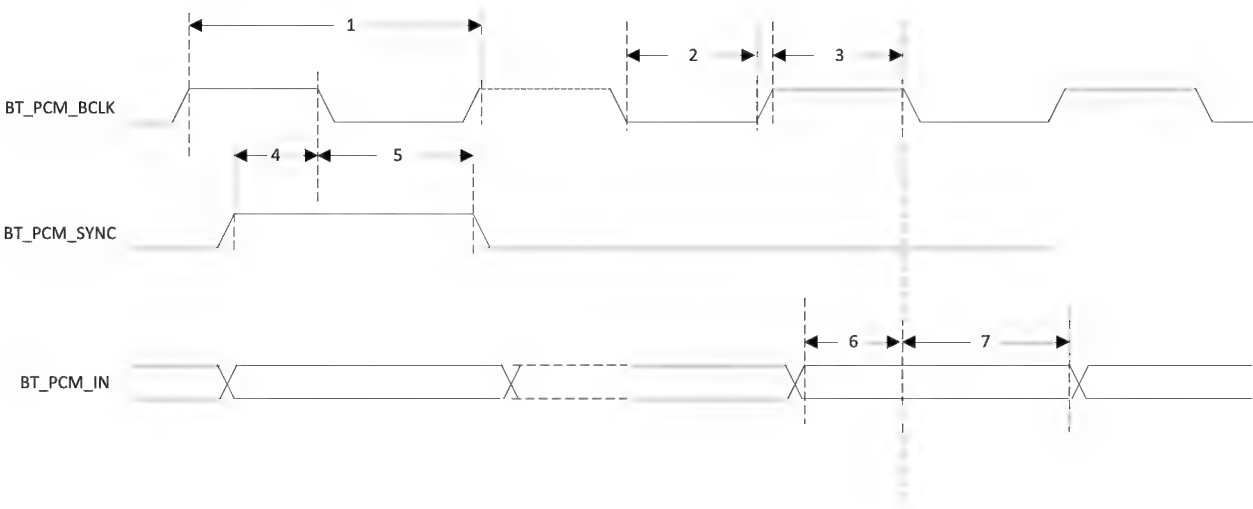


Table 16: PCM Burst Mode (Receive Only, Short Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	—	—	24	MHz
2	PCM bit clock low	20.8	—	—	ns
3	PCM bit clock high	20.8	—	—	ns
4	BT_PCM_SYNC setup	8	—	—	ns
5	BT_PCM_SYNC hold	8	—	—	ns
6	BT_PCM_IN setup	8	—	—	ns
7	BT_PCM_IN hold	8	—	—	ns

5.2.6.6 Long Frame Sync, Burst Mode

Figure 16: PCM Burst Mode Timing (Receive Only, Long Frame Sync)

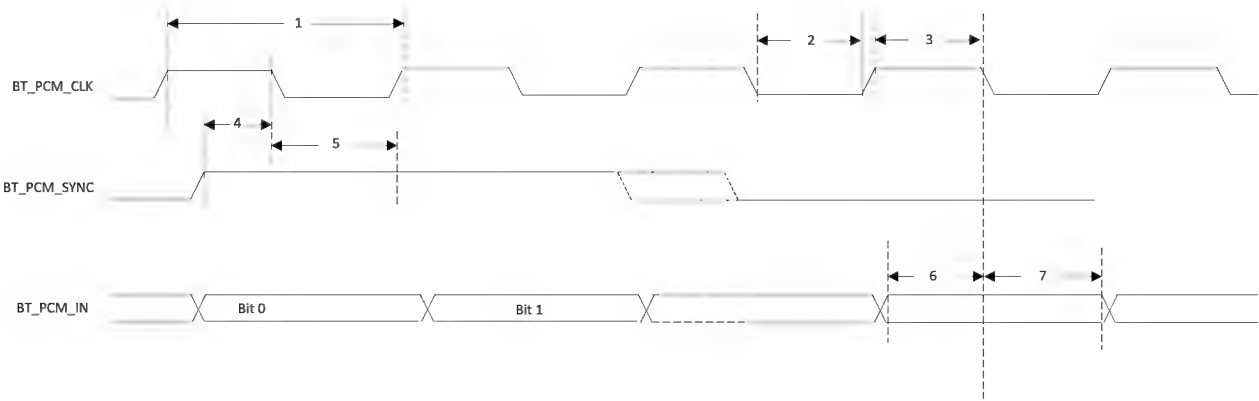


Table 17: PCM Burst Mode (Receive Only, Long Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	—	—	24	MHz
2	PCM bit clock low	20.8	—	—	ns
3	PCM bit clock high	20.8	—	—	ns
4	BT_PCM_SYNC setup	8	—	—	ns
5	BT_PCM_SYNC hold	8	—	—	ns
6	BT_PCM_IN setup	8	—	—	ns
7	BT_PCM_IN hold	8	—	—	ns

## 5.3 UART Interface

The BCM4375 UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth 5.0 UART HCI specification: H4, a custom Extended H4, and H5. The default baud rate is 115.2 Kbaud.

The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification ("Three-wire UART Transport Layer"). Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

The BCM4375 UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The BCM4375 UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within  $\pm 2\%$ .

**Table 18: Example of Common Baud Rates**

Desired Rate	Actual Rate	Error (%)
4000000	4000000	0.00
3692000	3692308	0.01
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19200	0.00
14400	14423	0.16
9600	9600	0.00

Figure 17: UART Timing

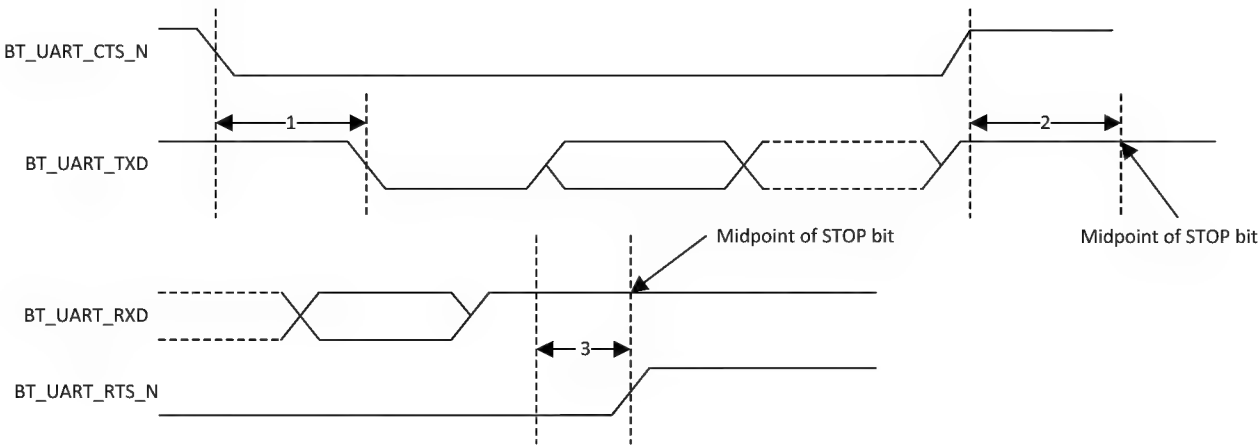


Table 19: UART Timing Specifications

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	Delay time, BT_UART_CTS_N low to BT_UART_TXD valid	—	—	1.5	Bit periods
2	Setup time, BT_UART_CTS_N high before midpoint of stop bit	—	—	0.5	Bit periods
3	Delay time, midpoint of stop bit to BT_UART_RTS_N high	—	—	0.5	Bit periods

## 5.4 I<sup>2</sup>S Interface

The BCM4375 supports an I<sup>2</sup>S digital audio port for Bluetooth audio. The I<sup>2</sup>S signals are:

- I<sup>2</sup>S clock: BT\_I2S\_CLK
- I<sup>2</sup>S Word Select: BT\_I2S\_WS
- I<sup>2</sup>S Data Out: BT\_I2S\_DO
- I<sup>2</sup>S Data In: BT\_I2S\_DI

BT\_I2S\_CLK and BT\_I2S\_WS become outputs in master mode and inputs in slave mode, whereas BT\_I2S\_DO always stays as an output. The channel word length is 16 bits, and the data is justified so that the MSB of the left-channel data is aligned with the MSB of the I<sup>2</sup>S bus, in accord with the I<sup>2</sup>S specification. The MSB of each data word is transmitted one bit clock cycle after the BT\_I2S\_WS transition, synchronous with the falling edge of the bit clock. Left-channel data is transmitted when BT\_I2S\_WS is low, and right-channel data is transmitted when BT\_I2S\_WS is high. Data bits sent by the BCM4375 are synchronized with the falling edge of BT\_I2S\_CLK and should be sampled by the receiver on the rising edge of BT\_I2S\_CLK.

The clock rate in master mode is either of the following:

48 kHz x 32 bits per frame = 1.536 MHz

48 kHz x 50 bits per frame = 2.400 MHz

The master clock is generated from the input reference clock using a N/M clock divider.

In the slave mode, any clock rate is supported to a maximum of 3.072 MHz.

## 5.4.1 I<sup>2</sup>S Timing

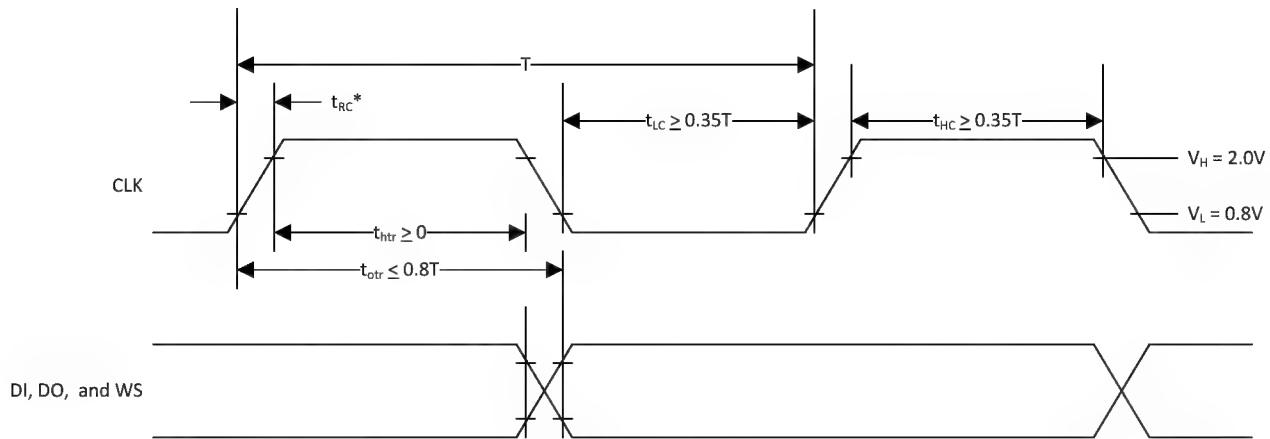
**NOTE:** Timing values specified in Table 20 are relative to high and low threshold levels.

**Table 20: Timing for I<sup>2</sup>S Transmitters and Receivers**

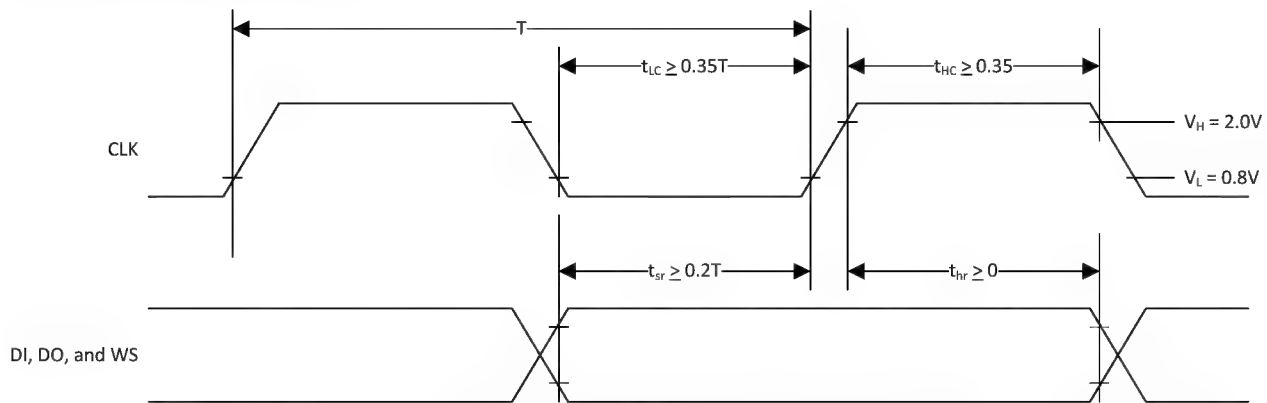
	Transmitter				Receiver				Notes
	Lower Limit		Upper Limit		Lower Limit		Upper Limit		
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Clock period T	T <sub>tr</sub>	—	—	—	T <sub>r</sub>	—	—	—	a
Master Mode: Clock generated by transmitter or receiver									
HIGH t <sub>HC</sub>	0.35T <sub>tr</sub>	—	—	—	0.35T <sub>tr</sub>	—	—	—	b
LOW t <sub>LC</sub>	0.35T <sub>tr</sub>	—	—	—	0.35T <sub>tr</sub>	—	—	—	b
Slave Mode: Clock accepted by transmitter or receiver									
HIGH t <sub>HC</sub>	—	0.35T <sub>tr</sub>	—	—	—	0.35T <sub>tr</sub>	—	—	c
LOW t <sub>LC</sub>	—	0.35T <sub>tr</sub>	—	—	—	0.35T <sub>tr</sub>	—	—	c
Rise time t <sub>RC</sub>	—	—	0.15T <sub>tr</sub>	—	—	—	—	—	d
Transmitter									
Delay t <sub>dtr</sub>	—	—	—	0.8T	—	—	—	—	e
Hold time t <sub>htr</sub>	0	—	—	—	—	—	—	—	d
Receiver									
Setup time t <sub>sr</sub>	—	—	—	—	—	0.2T <sub>r</sub>	—	—	f
Hold time t <sub>hr</sub>	—	—	—	—	—	0	—	—	f

- The system clock period T must be greater than  $T_{tr}$  and  $T_r$  because both the transmitter and receiver have to be able to handle the data transfer rate.
- At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason,  $t_{HC}$  and  $t_{LC}$  are specified with respect to T.
- In slave mode, the transmitter and receiver need a clock signal with minimum high and low periods so that they can detect the signal. So long as the minimum periods are greater than  $0.35T_r$ , any clock that meets the requirements can be used.
- Because the delay ( $t_{dtr}$ ) and the maximum transmitter speed (defined by  $T_{tr}$ ) are related, a fast transmitter driven by a slow clock edge can result in  $t_{dtr}$  not exceeding  $t_{RC}$  which means  $t_{htr}$  becomes zero or negative. Therefore, the transmitter has to guarantee that  $t_{htr}$  is greater than or equal to zero, so long as the clock rise-time  $t_{RC}$  is not more than  $t_{RCmax}$ , where  $t_{RCmax}$  is not less than  $0.15T_{tr}$ .
- To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.
- The data setup and hold time must not be less than the specified receiver setup and hold time.

**NOTE:** The time periods specified in Figure 18 and Figure 19 are defined by the transmitter speed. The receiver specifications must match transmitter performance.

**Figure 18: I<sup>2</sup>S Transmitter Timing**

T = Clock period

 $T_{tr}$  = Minimum allowed clock period for transmitter $T = T_{tr}$ \*  $t_{RC}$  is only relevant for transmitters in slave mode.**Figure 19: I<sup>2</sup>S Receiver Timing**

T = Clock period

 $T_r$  = Minimum allowed clock period for transmitter $T > T_r$

## Chapter 6: WLAN Global Functions and Interfaces

### 6.1 WLAN CPU and Memory Subsystem

The BCM4375 WLAN section includes an integrated ARM Cortex-R4 32-bit processor with internal RAM and ROM. The on-chip memory for the CPU includes 1600 KB SRAM and 1216 KB ROM.

### 6.2 One-Time Programmable Memory

Various hardware configuration parameters may be stored in an internal one-time programmable (OTP) memory, which is read by the system software after device reset. In addition, customer-specific parameters, including the system vendor ID and the MAC address can be stored, depending on the specific board design. Up to 1150 bytes of user-accessible OTP are available.

The initial state of all bits in an unprogrammed OTP device is 0. After any bit is programmed to a 1, it cannot be reprogrammed to 0. The entire OTP array can be programmed in a single write cycle using a utility provided with the Broadcom WLAN manufacturing test tools. Alternatively, multiple write cycles can be used to selectively program specific bytes, but only bits which are still in the 0 state can be altered during each programming cycle.

Prior to OTP programming, all values should be verified using the appropriate editable nvram.txt file, which is provided with the reference board design package.

### 6.3 GPIO Interface

The BCM4375 has 21 general-purpose I/O (GPIO) pins in the WLAN section that can be used to connect to various external devices.

Upon power-up and reset, these pins become tristated. Subsequently, they can be programmed to be either input or output pins via the GPIO control register. In addition, the GPIO pins can be assigned to various other functions, see [Table 39, GPIO Alternative Signal Functions](#).

## 6.4 External Coexistence Interface

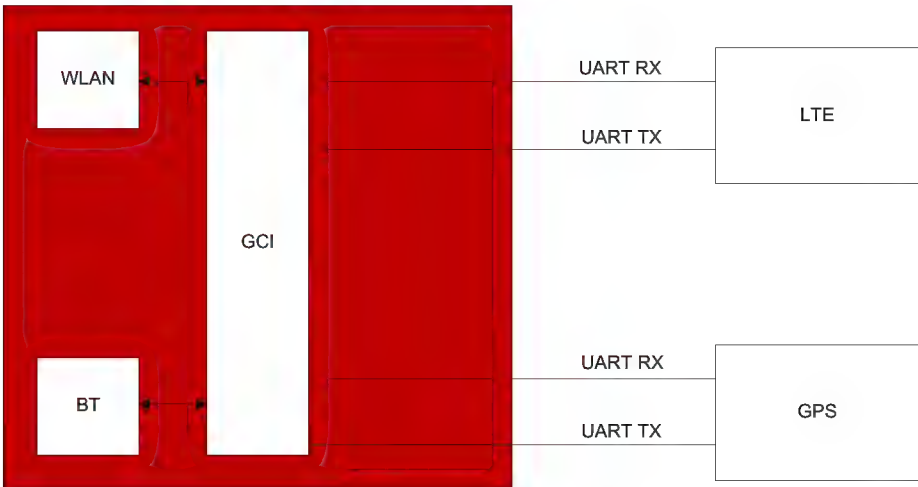
An external handshake interface is available to enable signaling between the BCM4375 and an external collocated wireless device to manage wireless medium sharing for optimal performance.

Figure 20 shows the BCM4375 coexistence interface (including UART). See Table 39, GPIO Alternative Signal Functions for further details on multiplexed signals, such as the GPIO pins.

Baud rates are derived from crystal clock. For rates higher than [Crystal\_Frequency /16] the baud rate is an integer divide of the crystal frequency. For 37.4 MHz crystal:

Division	XTAL	Baud rate (Mbps)
12	37.4/12	3.116667
13	37.4/13	2.876923
14	37.4/14	2.671429
15	37.4/15	2.493333
16	37.4/16	2.3375

Figure 20: Multipoint Global Coexistence Interface



## 6.5 Debug UART Interface

One 2-wire UART interface can be enabled by software as an alternate function on GPIO pins. Refer to Table 39, GPIO Alternative Signal Functions. Provided primarily for debugging during development, this UART enables the BCM4375 to operate as RS-232 data termination equipment (DTE) for exchanging and managing data with other serial devices. It is compatible with the industry standard 16550 UART, and provides a FIFO size of 64 × 8 in each direction.

## 6.6 FAST UART Interface

A high-speed 4-wire CTS/RTS UART interface can be enabled by software as an alternate function on GPIO pins. Refer to [Table 39, GPIO Alternative Signal Functions](#). Provided primarily for control word exchange, this UART enables the chip to operate as RS-232 data termination equipment (DTE) for exchanging and managing data with other serial devices. It is compatible with the industry standard 16550 UART, and provides a FIFO size of 64 × 8 in each direction.

## 6.7 BSC Interface

A proprietary Broadcom Serial Control (BSC, an I<sup>2</sup>C-compatible interface) slave interface is available, as an alternate function on the GPIO lines, which supports data transfer rates up to 3.4 Mbps in high-speed mode. This can be primarily used to transfer data to a sensor hub in the host system. This interface supports 7-bit and 10-bit device addressing and an interrupt to the processor. Based on the device address matching, a device can be brought out of low-power state using this interface. This interface provides an internal FIFO depth of 32 bytes for both TX and RX with the ability to filter glitches on the clock and data lines.

## 6.8 JTAG/SWD Interface

The BCM4375 supports IEEE 1149.1 JTAG boundary scan and reduced pin-count SWD mode to access the chip's internal blocks and backplane for system bring-up and debugging. This interface allows Broadcom to assist customers with proprietary debug and characterization test tools. It is highly recommended that access is provided to at least the SWD pins by using either test points or a header on all PCB designs.

The SWD interface uses two of the JTAG signals: TMS for bidirectional data (SWDIO) and TCK for the clock (SWCLK). The debug access port (DAP) embedded in the ARM processor supports both SWD and JTAG interfaces and can be switched from one to the other via a specific sequence on the TMS/SWD lines. In addition to the ARM debug interface, an internal JTAG master on the DAP allows access to test access points (TAPs) in the BCM4375 for hardware debugging.

Refer to [Table 39, GPIO Alternative Signal Functions](#) for JTAG pin assignments.

## 6.8.1 JTAG Timing

Table 21: JTAG Timing Characteristics

Signal Name	Period	Output Maximum	Output Minimum	Setup	Hold
TCK	125 ns	—	—	—	—
TDI	—	—	—	20 ns	0 ns
TMS	—	—	—	20 ns	0 ns
TDO	—	100 ns	0 ns	—	—
JTAG_TRST	250 ns	—	—	—	—

## 6.8.2 SWD Timing

The probe outputs data to SWDIO (TMS) on the falling edge of SWDCLK (TCK) and captures data from SWDIO on the rising edge of SWDCLK. The target outputs data to SWDIO on the rising edge of SWDCLK and captures data from SWDIO on the rising edge of SWDCLK.

SWD timing is shown through the combination of [Figure 21](#) and [Table 22](#).

Figure 21: SWD Read and Write Timing

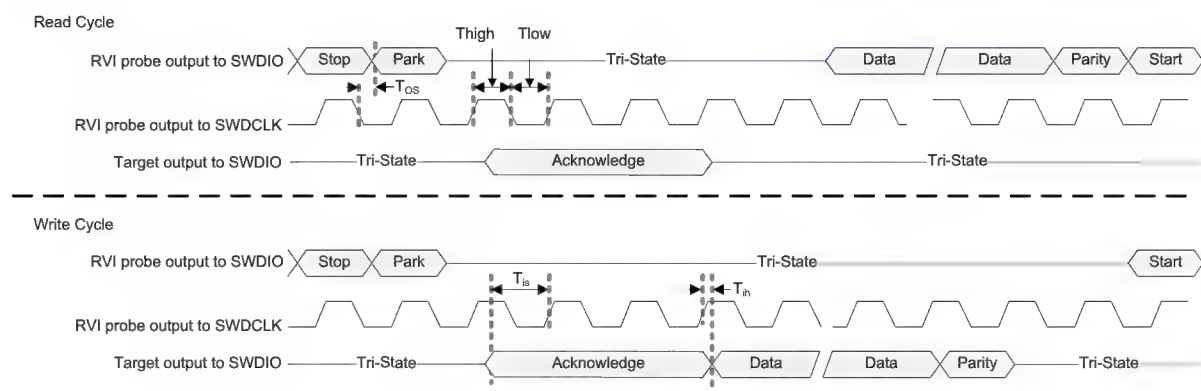


Table 22: SWD Read and Write Timing Parameters

Parameter	Description	Min.	Max.	Unit
T <sub>cyc</sub>	SWDCLK cycle time	125	—	ns
T <sub>high</sub>	SWDCLK high period	50	—	ns
T <sub>low</sub>	SWDCLK low period	50	—	ns
T <sub>os</sub>	SWDIO output skew to the falling edge of SWDCLK	–5	5	ns
T <sub>is</sub>	Input setup time between SWDIO and the rising edge of SWDCLK	20	—	ns
T <sub>ih</sub>	Input hold time between SWDIO and the rising edge of SWDCLK	0	100	ns

## 6.9 PCI Express Interface

The PCI Express (PCIe) core on the BCM4375 is a high-performance serial I/O interconnect that is protocol compliant and electrically compatible with the *PCI Express Base Specification v3.0* running at Gen2 speeds.

Table 23 provides the PCIe interface parameters.

**Table 23: PCI Express Interface Parameters**

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
<b>General<sup>a</sup></b>						
Baud rate	BPS	—	—	5	—	Gbaud
Reference clock peak-to-peak differential <sup>b</sup>	Vref	LVPECL, AC coupled	0.95	—	—	V
<b>Receiver</b>						
Differential termination	ZRX-DIFF-DC	Differential termination	80	100	120	Ω
DC impedance	ZRX-DC	DC common-mode impedance	40	50	60	Ω
Powered down termination (POS)	ZRX-HIGH-IMP-DC-POS	Power-down or RESET high impedance	100k	—	—	Ω
Powered down termination (NEG)	ZRX-HIGH-IMP-DC-NEG	Power-down or RESET high impedance	1k	—	—	Ω
Input voltage	VRX-DIFFp-p	AC coupled, differential p-p	175	—	—	mV
Jitter tolerance	TRX-EYE	Minimum receiver eye width	0.4	—	—	UI
Differential return loss	RLRX-DIFF	Differential return loss	10	—	—	dB
Common-mode return loss	RLRX-CM	Common-mode return loss	6	—	—	dB
Unexpected electrical idle enter detect threshold integration time	TRX-IDEL-DET-DIFF-ENTERTIME	An unexpected electrical idle must be recognized no longer than this time to signal an unexpected idle condition.	—	—	10	ms
Signal detect threshold	VRX-IDLE-DET-DIFFp-p	Electrical idle detect threshold	65	—	175	mV
<b>Transmitter</b>						
Output voltage	VTX-DIFFp-p	Differential p-p, programmable in 16 steps	0.8	—	1200	mV
Output voltage rise time	VTX-RISE	20% to 80%	0.125 (2.5 GT/s) 0.15 (5 GT/s)	—	—	UI
Output voltage fall time	VTX-FALL	80% to 20%	0.125 (2.5 GT/s) 0.15 (5 GT/s)	—	—	UI
RX detection voltage swing	VTX-RCV-DETECT	The amount of voltage change allowed during receiver detection.	—	—	600	mV

**Table 23: PCI Express Interface Parameters (Continued)**

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
TX AC peak common-mode voltage (5 GT/s)	VTX-CM-AC-PP	TX AC common mode voltage (5 GT/s)	—	—	100	mV
TX AC peak common-mode voltage (2.5 GT/s)	VTX-CM-AC-P	TX AC common mode voltage (2.5 GT/s)	—	—	20	mV
Absolute delta of DC common-mode voltage during L0 and electrical idle	VTX-CM-DC-ACTIVE-IDLE-DELTA	Absolute delta of DC common-mode voltage during L0 and electrical idle.	0	—	100	mV
Absolute delta of DC common-mode voltage between D+ and D-	VTX-CM-DC-LINE-DELTA	DC offset between D+ and D-	0	—	25	mV
Electrical idle differential peak output voltage	VTX-IDLE-DIFF-AC-p	Peak-to-peak voltage	0	—	20	mV
TX short circuit current	ITX-SHORT	Current limit when TX output is shorted to ground.	—	—	90	mA
DC differential TX termination	ZTX-DIFF-DC	Low impedance defined during signaling (parameter is captured for 5.0 GHz by RLTX-DIFF)	80	—	120	$\Omega$
Differential return loss	RLTX-DIFF	Differential return loss	10 (min) for 0.05: 1.25 GHz	—	—	dB
Common-mode return loss	RLTX-CM	Common-mode return loss	6	—	—	dB
TX eye width	TTX-EYE	Minimum TX eye width	0.75	—	—	UI

- a. For out-of-band PCIe signal specification, refer to [Table 3, Recommended Operating Conditions and DC Characteristics](#).
- b. The reference clock inputs comply with the requirements of the *PCI Express CEM v2.0 Specification*.

## Chapter 7: Bluetooth RF Specifications

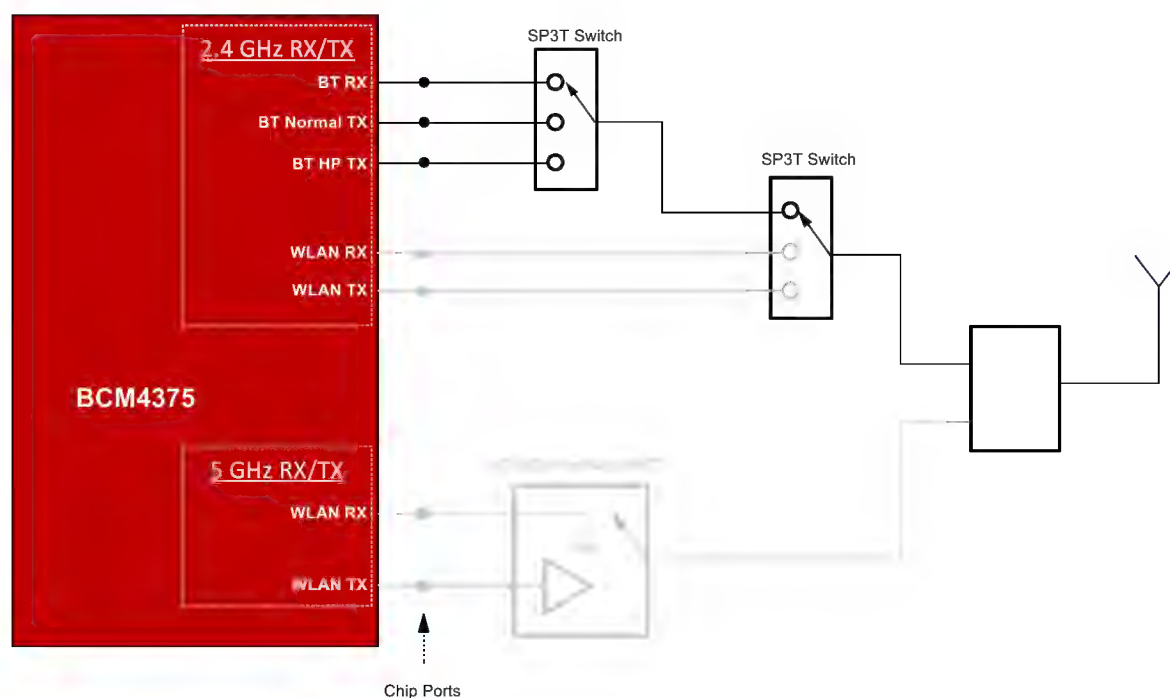
**NOTE:** Values in this data sheet are design goals and are subject to change based on device characterization results.

Unless otherwise stated, limit values apply for the conditions specified in [Table 2, Environmental Ratings](#) and [“Recommended Operating Conditions and DC Characteristics”](#) on page 7.

Typical values apply for the following conditions:

- VBAT = 3.6V
- Ambient temperature +25°C

**Figure 22: Port Locations for Bluetooth Testing**



**NOTE:** The specifications in [Table 24](#) are measured at the chip port input, unless otherwise defined.

**Table 24: Bluetooth Receiver RF Specifications**

Parameter	Conditions	Minimum	Typical	Maximum	Unit
<b>General</b>					
Frequency range	—	2402	—	2480	MHz
Receive sensitivity in high performance mode (dLNA_HP) with dirty transmit off	1 Mbps, GFSK BDR, 0.1% BER	—	−95	—	dBm
	2 Mbps, $\pi/4$ -DQPSK EDR-2, 0.01% BER	—	−97	—	dBm
	3 Mbps, 8-DQPSK EDR-3, 0.01% BER	—	−91	—	dBm
Receive sensitivity in low power mode (dLNA_LP) with dirty transmit off	1 Mbps, GFSK BDR, 0.1% BER	—	−95	—	dBm
	2 Mbps, $\pi/4$ -DQPSK EDR-2, 0.01% BER	—	−97	—	dBm
	3 Mbps, 8-DQPSK EDR-3, 0.01% BER	—	−91	—	dBm

**Table 24: Bluetooth Receiver RF Specifications (Continued)**

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Receive sensitivity: LELR, BLE, and LE2 (dLNA_LP and sLNA_LP) with dirty transmit off.	125 Kbps, LELR, 30.8% PER	—	–110	–107	dBm
	500 Kbps, LELR, 30.8% PER	—	–105	–102	dBm
	1 Mbps, GFSK BLE, 30.8% PER	—	–98	–95	dBm
	2 Mbps, LE2, 30.8% PER	—	–95	–92	dBm
Input IP3 (max. LNA gain)	—	–24	—	—	dBm
Maximum input at chip port	Without damaging the chip	—	—	13	dBm
Maximum receive level	BDR, EDR-2, EDR-3	–17	—	—	dBm
	BLE, LELR, LE2	–7	—	—	dBm
<b>RX LO Leakage</b>					
2.4 GHz band	—	—	–90	—	dBm
<b>Interference Performance <sup>a, b</sup></b>					
C/I co-channel	GFSK, 0.1% BER	—	—	11	dB
C/I 1 MHz adjacent channel	GFSK, 0.1% BER	—	—	0	dB
C/I 2 MHz adjacent channel	GFSK, 0.1% BER	—	—	–30	dB
C/I ≥ 3 MHz adjacent channel	GFSK, 0.1% BER	—	—	–40	dB
C/I image channel	GFSK, 0.1% BER	—	—	–9	dB
C/I 1-MHz adjacent to image channel	GFSK, 0.1% BER	—	—	–20	dB
C/I co-channel	$\pi/4$ -DQPSK, 0.1% BER	—	—	13	dB
C/I 1 MHz adjacent channel	$\pi/4$ -DQPSK, 0.1% BER	—	—	0	dB
C/I 2 MHz adjacent channel	$\pi/4$ -DQPSK, 0.1% BER	—	—	–30	dB
C/I ≥ 3 MHz adjacent channel	$\pi/4$ -DQPSK, 0.1% BER	—	—	–40	dB
C/I image channel	$\pi/4$ -DQPSK, 0.1% BER	—	—	–7	dB
C/I 1 MHz adjacent to image channel	$\pi/4$ -DQPSK, 0.1% BER	—	—	–20	dB
C/I co-channel	8-DPSK, 0.1% BER	—	—	21	dB
C/I 1 MHz adjacent channel	8-DPSK, 0.1% BER	—	—	5	dB
C/I 2 MHz adjacent channel	8-DPSK, 0.1% BER	—	—	–25	dB
C/I ≥ 3 MHz adjacent channel	8-DPSK, 0.1% BER	—	—	–33	dB
C/I Image channel	8-DPSK, 0.1% BER	—	—	0	dB
C/I 1 MHz adjacent to image channel	8-DPSK, 0.1% BER	—	—	–13	dB
<b>Out-of-Band Blocking Performance (CW) <sup>b</sup></b>					
30–2000 MHz	0.1% BER	—	–10	—	dBm
2000–2399 MHz	0.1% BER	—	–27	—	dBm
2498–3000 MHz	0.1% BER	—	–27	—	dBm
3000 MHz–12.75 GHz	0.1% BER	—	–10	—	dBm
<b>Out-of-Band Blocking Performance, Modulated Interferer <sup>c d</sup></b>					
<b>GFSK (1 Mbps)</b>					
698–716 MHz	WCDMA	—	–5	—	dBm
776–794 MHz	WCDMA	—	–5	—	dBm

Table 24: Bluetooth Receiver RF Specifications (Continued)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
824–849 MHz	GSM850	—	–5	—	dBm
824–849 MHz	WCDMA	—	–5	—	dBm
880–915 MHz	E-GSM	—	–5	—	dBm
880–915 MHz	WCDMA	—	–5	—	dBm
1710–1785 MHz	GSM1800	—	–9	—	dBm
1710–1785 MHz	WCDMA	—	–11	—	dBm
1850–1910 MHz	GSM1900	—	–11	—	dBm
1850–1910 MHz	WCDMA	—	–13	—	dBm
1880–1920 MHz	TD-SCDMA	—	–14	—	dBm
1920–1980 MHz	WCDMA	—	–14	—	dBm
2010–2025 MHz	TD-SCDMA	—	–16	—	dBm
2500–2570 MHz	WCDMA	—	–21	—	dBm
2310 MHz	LTE band 40, TDD, 20 MHz BW	—	–29	—	dBm
2330 MHz	LTE band 40, TDD, 20 MHz BW	—	–30	—	dBm
2350 MHz	LTE band 40, TDD, 20 MHz BW	—	–31	—	dBm
2370 MHz	LTE band 40, TDD, 20 MHz BW	—	–31	—	dBm
2510 MHz	LTE band 7, FDD, 20 MHz BW	—	–28	—	dBm
2530 MHz	LTE band 7, FDD, 20 MHz BW	—	–27	—	dBm
2550 MHz	LTE band 7, FDD, 20 MHz BW	—	–27	—	dBm
2570 MHz	LTE band 7, FDD, 20 MHz BW	—	–26	—	dBm
2570–2620 MHz <sup>e</sup>	Band 38	—	–23	—	dBm
2545–2575 MHz <sup>f</sup>	XGP Band	—	–24	—	dBm
3400–3600 MHz	LTE band 42, TDD, 20 MHz BW	—	–14	—	dBm
3600–3800 MHz	LTE band 43, TDD, 20 MHz BW	—	–11	—	dBm
<b><math>\pi/4</math>-DPSK (2 Mbps)</b>					
698–716 MHz	WCDMA	—	–5	—	dBm
776–794 MHz	WCDMA	—	–5	—	dBm
824–849 MHz	GSM850	—	–5	—	dBm
824–849 MHz	WCDMA	—	–5	—	dBm
880–915 MHz	E-GSM	—	–5	—	dBm
880–915 MHz	WCDMA	—	–5	—	dBm
1710–1785 MHz	GSM1800	—	–9	—	dBm
1710–1785 MHz	WCDMA	—	–11	—	dBm
1850–1910 MHz	GSM1900	—	–11	—	dBm
1850–1910 MHz	WCDMA	—	–13	—	dBm
1880–1920 MHz	TD-SCDMA	—	–14	—	dBm
1920–1980 MHz	WCDMA	—	–14	—	dBm
2010–2025 MHz	TD-SCDMA	—	–16	—	dBm
2500–2570 MHz	WCDMA	—	–21	—	dBm
2310 MHz	LTE band 40, TDD, 20 MHz BW	—	–29	—	dBm
2330 MHz	LTE band 40, TDD, 20 MHz BW	—	–30	—	dBm
2350 MHz	LTE band 40, TDD, 20 MHz BW	—	–31	—	dBm

**Table 24: Bluetooth Receiver RF Specifications (Continued)**

Parameter	Conditions	Minimum	Typical	Maximum	Unit
2370 MHz	LTE band 40, TDD, 20 MHz BW	—	–31	—	dBm
2510 MHz	LTE band 7, FDD, 20 MHz BW	—	–28	—	dBm
2530 MHz	LTE band 7, FDD, 20 MHz BW	—	–27	—	dBm
2550 MHz	LTE band 7, FDD, 20 MHz BW	—	–27	—	dBm
2570 MHz	LTE band 7, FDD, 20 MHz BW	—	–26	—	dBm
2570–2620 MHz <sup>e</sup>	Band 38	—	–23	—	dBm
2545–2575 MHz <sup>f</sup>	XGP Band	—	–24	—	dBm
3400-3600 MHz	LTE band 42, TDD, 20 MHz BW	—	–14	—	dBm
3600-3800 MHz	LTE band 43, TDD, 20 MHz BW	—	–11	—	dBm
<b>8-DPSK (3 Mbps)</b>					
698-716 MHz	WCDMA	—	–5	—	dBm
776-794 MHz	WCDMA	—	–5	—	dBm
824-849 MHz	GSM850	—	–5	—	dBm
824-849 MHz	WCDMA	—	–5	—	dBm
880-915 MHz	E-GSM	—	–5	—	dBm
880-915 MHz	WCDMA	—	–5	—	dBm
1710-1785 MHz	GSM1800	—	–9	—	dBm
1710-1785 MHz	WCDMA	—	–11	—	dBm
1850-1910 MHz	GSM1900	—	–11	—	dBm
1850-1910 MHz	WCDMA	—	–13	—	dBm
1880-1920 MHz	TD-SCDMA	—	–14	—	dBm
1920-1980 MHz	WCDMA	—	–14	—	dBm
2010-2025 MHz	TD-SCDMA	—	–16	—	dBm
2500-2570 MHz	WCDMA	—	–21	—	dBm
2310 MHz	LTE band 40, TDD, 20 MHz BW	—	–29	—	dBm
2330 MHz	LTE band 40, TDD, 20 MHz BW	—	–30	—	dBm
2350 MHz	LTE band 40, TDD, 20 MHz BW	—	–31	—	dBm
2370 MHz	LTE band 40, TDD, 20 MHz BW	—	–31	—	dBm
2510 MHz	LTE band 7, FDD, 20 MHz BW	—	–28	—	dBm
2530 MHz	LTE band 7, FDD, 20 MHz BW	—	–27	—	dBm
2550 MHz	LTE band 7, FDD, 20 MHz BW	—	–27	—	dBm
2570 MHz	LTE band 7, FDD, 20 MHz BW	—	–26	—	dBm
2570–2620 MHz <sup>e</sup>	Band 38	—	–23	—	dBm
2545–2575 MHz <sup>f</sup>	XGP Band	—	–24	—	dBm
3400-3600 MHz	LTE band 42, TDD, 20 MHz BW	—	–14	—	dBm
3600-3800 MHz	LTE band 43, TDD, 20 MHz BW	—	–11	—	dBm

**Table 24: Bluetooth Receiver RF Specifications (Continued)**

Parameter	Conditions	Minimum	Typical	Maximum	Unit
<b>Spurious Emissions <sup>b</sup></b>					
30 MHz–1 GHz		—	–95	–62	dBm
1–12.75 GHz		—	–70	–47	dBm
851–894 MHz		—	–147	—	dBm/Hz
925–960 MHz		—	–147	—	dBm/Hz
1805–1880 MHz		—	–147	—	dBm/Hz
1930–1990 MHz		—	–147	—	dBm/Hz
2110–2170 MHz		—	–147	—	dBm/Hz

a. The maximum value represents the actual Bluetooth specification required for Bluetooth qualification as defined in the version 4.1 specification.

b. Applicable for all RX.

c. Applicable for dLNA\_HP.

d. The Bluetooth sensitivity levels for 1 Mbps, 2 Mbps, and 3 Mbps operation are –90.5 dBm, –92.5 dBm, and –86.5 dBm, respectively, in the presence of the blockers indicated.

e. Interferer: 2580 MHz, BW = 10 MHz, measured at 2480 MHz.

f. Interferer: 2555 MHz, BW = 10 MHz, measured at 2480 MHz.

**NOTE:** The specifications in this table are measured at the Bluetooth chip port output, unless otherwise defined.

**Table 25: Bluetooth Transmitter RF Specifications**

Parameter	Conditions	Min.	Typical	Max.	Unit
<b>General – BT Output Power Mode</b>					
Frequency range	—	2402	—	2480	MHz
TX output power requirement in BT normal-power mode: TX power at chip output that meets <i>Bluetooth Test Specification RF.TS.4.0.0 ACP/EVM</i> requirements.	BDR, GFSK	11.5	14	15.5	dBm
	EDR-2, $\pi/4$ -DQPSK	7.5	10	11.5	dBm
	EDR-3, 8-DPSK	7.5	10	11.5	dBm
	BLE, GFSK	11.5	14	15.5	dBm
	LE2	11.5	14	15.5	dBm
	LELR	11.5	14	15.5	dBm
TX output power requirement in BT high-power mode: TX power at chip output that meets <i>Bluetooth Test Specification RF.TS.4.0.0 ACP/EVM</i> requirements.	BDR, GFSK	17.5	20	21.5	dBm
	EDR-2, $\pi/4$ -DQPSK	11.5	14	15.5	dBm
	EDR-3, 8-DPSK	11.5	14	15.5	dBm
	BLE, GFSK	17.5	20	21.5	dBm
	LE2	17.5	20	21.5	dBm
	LELR	17.5	20	21.5	dBm
Chip shall meet all ACP/EVM requirements specified in <i>Bluetooth Test Specification RF.TS.4.0.0</i>	—	–2	—	2	dB
Power control step	—	—	4	—	dB
Power control accuracy over process	BDR, EDR-2, EDR-3	–2	—	1	dB
TX power control dynamic range	Need to support BT normal power mode and BT high power mode	32	—	—	dB
Gain control step	For setting output power	—	—	0.25	dB
Return loss at chip port TX	$Z_0 = 50\Omega$ , across the TX dynamic range	—	8	—	dB
<b>NOTE:</b> Output power is with TCA and TSSI enabled.					
<b>GFSK In-Band Spurious Emissions</b>					
–20 dBc BW	—	—	0.93	1	MHz
<b>EDR In-Band Spurious Emissions</b>					
1.0 MHz <  M – N  < 1.5 MHz	M – N = the frequency range for which the spurious emission is measured relative to the transmit center frequency.	—	–38	–26	dBc
1.5 MHz <  M – N  < 2.5 MHz		—	–27	–20	dBm
M – N  ≥ 2.5 MHz <sup>a</sup>		—	–43	–40	dBm

**Table 25: Bluetooth Transmitter RF Specifications (Continued)**

Parameter	Conditions	Min.	Typical	Max.	Unit
<b>Out-of-Band Spurious Emissions</b>					
TX harmonics (HD2, HD3, HD4) in BT normal-power mode	HD2 with TX at full power	—	—	–19	dBm/MHz
	HD3 with TX at full power	—	—	–30	dBm/MHz
	HD4 with TX at full power	—	—	–44	dBm/MHz
TX harmonics (HD2, HD3, HD4) in BT high-power mode	HD2 with TX at full power	—	—	–13	dBm/MHz
	HD3 with TX at full power	—	—	–17	dBm/MHz
	HD4 with TX at full power	—	—	–30	dBm/MHz
Transmit spurious in BT normal-power and high-power modes	30 MHz to 1 GHz	—	—	–50	dBm/MHz
	1 GHz to 12.75 GHz	—	—	–50	dBm/MHz
	1.8 GHz to 1.9 GHz	—	—	–50	dBm/MHz
	5.15 GHz to 5.3 GHz	—	—	–50	dBm/MHz
VCO spurs at the fundamental frequency over the full TX dynamic range	BT normal-power mode	—	—	–35	dBm/MHz
	BT high-power mode	—	—	–32	dBm/MHz
<b>GPS Band Spurious Emissions</b>					
Spurious emissions	—	—	–160	—	dBm
<b>Out-of-Band Noise Floor <sup>b</sup></b>					
65–108 MHz	FM RX	—	–165	—	dBm/Hz
776–794 MHz	CDMA2000	—	–163	—	dBm/Hz
869–960 MHz	cdmaOne, GSM850	—	–163	—	dBm/Hz
925–960 MHz	E-GSM	—	–163	—	dBm/Hz
1570–1580 MHz	GPS	—	–160	—	dBm/Hz
1805–1880 MHz	GSM1800	—	–154	—	dBm/Hz
1930–1990 MHz	GSM1900, cdmaOne, WCDMA	—	–152	—	dBm/Hz
2110–2170 MHz	WCDMA	—	–145	—	dBm/Hz
2500–2570 MHz	Band 7	—	–133	—	dBm/Hz
2300–2400 MHz	Band 40	—	–132	—	dBm/Hz
2570–2620 MHz	Band 38	—	–135	—	dBm/Hz
2545–2575 MHz	XGP Band	—	–134	—	dBm/Hz

a. The typical number is measured at  $\pm 3$  MHz offset.

b. Transmitted power in cellular and FM bands at the antenna port. See [Figure 22](#) for the port location.

**Table 26: Local Oscillator Performance**

Parameter	Minimum	Typical	Maximum	Unit
<b>LO Performance</b>				
Lock time	—	72	—	μs
Initial carrier frequency tolerance	—	±25	±75	kHz
<b>Frequency Drift <sup>a</sup></b>				
DH1 packet	—	±8	±25	kHz
DH3 packet	—	±8	±40	kHz
DH5 packet	—	±8	±40	kHz
Drift rate	—	5	20	kHz/50 μs
<b>Frequency Deviation<sup>a</sup></b>				
00001111 sequence in payload <sup>b</sup>	140	155	175	kHz
10101010 sequence in payload <sup>c</sup>	115	140	—	kHz
Channel spacing	—	1	—	MHz

a. Applicable to BT nominal TX, BT HP TX, and BT 0 dBm TX.

b. This pattern represents an average deviation in payload.

c. Pattern represents the maximum deviation in payload for 99.9% of all frequency deviations.

## Chapter 8: WLAN RF Specifications

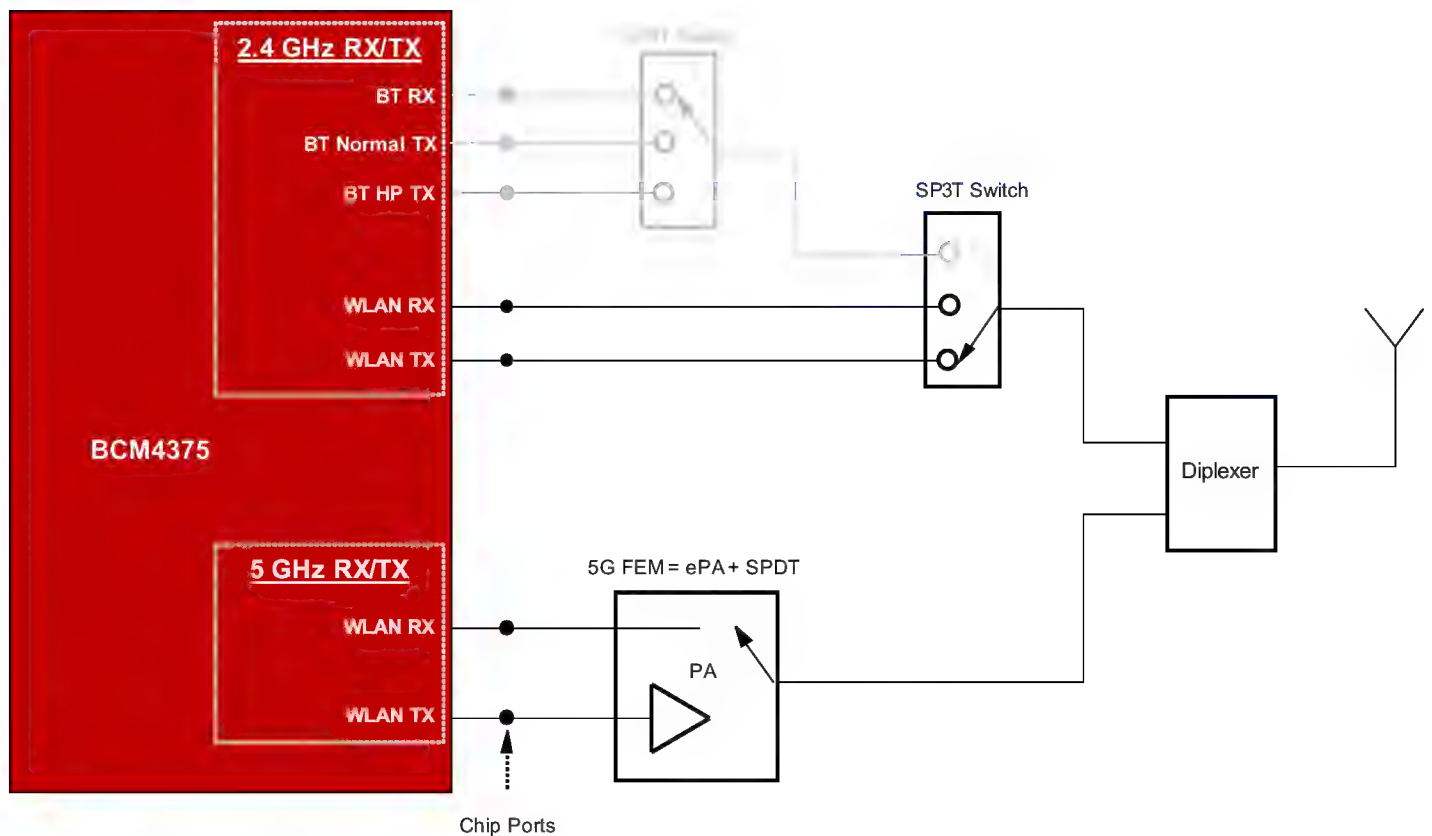
### 8.1 Introduction

The BCM4375 includes an integrated dual-band direct conversion radio that supports the 2.4 GHz and the 5 GHz bands. This section describes the RF characteristics of the 2.4 GHz and 5 GHz radios.

**NOTE:** Values in this section of the data sheet are design goals and are subject to change based on the results of device characterization.

Unless otherwise stated, limit values apply for the conditions specified in [Table 2, Environmental Ratings](#) and [Table 3, Recommended Operating Conditions and DC Characteristics](#). Typical values apply for an ambient temperature +25°C.

Figure 23: Port Locations for WLAN Testing



## 8.2 2.4 GHz Band General RF Specifications

Table 27: 2.4 GHz Band General RF Specifications

Item	Condition	Minimum	Typical	Maximum	Unit
TX/RX switch time	Including TX ramp down	—	—	5	µs
RX/TX switch time	Including TX ramp up	—	—	2	µs
Power-up and power-down ramp time	DSSS/CCK modulations	—	—	< 2	µs

## 8.3 WLAN 2.4 GHz Receiver Performance Specifications

**NOTE:** The values in Table 28 are specified at the chip RF port unless otherwise noted.

Table 28: WLAN 2.4 GHz Receiver Performance Specifications

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
Frequency range	—	2400	—	2500	MHz
RX sensitivity IEEE 802.11b	1 Mbps DSSS	—	−100.4	—	dBm
	2 Mbps DSSS	—	−97.2	—	dBm
	5.5 Mbps DSSS	—	−94.4	—	dBm
	11 Mbps DSSS	—	−91.4	—	dBm
SISO RX sensitivity IEEE 802.11g (10% PER for 1024 octet PSDU)	6 Mbps OFDM	—	−95	—	dBm
	9 Mbps OFDM	—	−93.9	—	dBm
	12 Mbps OFDM	—	−93	—	dBm
	18 Mbps OFDM	—	−90.4	—	dBm
	24 Mbps OFDM	—	−87.4	—	dBm
	36 Mbps OFDM	—	−84.1	—	dBm
	48 Mbps OFDM	—	−79.7	—	dBm
	54 Mbps OFDM	—	−78.2	—	dBm
MIMO RX sensitivity IEEE 802.11g (10% PER for 1024 octet PSDU)	6 Mbps OFDM	—	−97	—	dBm/core
	9 Mbps OFDM	—	−95.9	—	dBm/core
	12 Mbps OFDM	—	−95	—	dBm/core
	18 Mbps OFDM	—	−93.4	—	dBm/core
	24 Mbps OFDM	—	−90.4	—	dBm/core
	36 Mbps OFDM	—	−87.1	—	dBm/core
	48 Mbps OFDM	—	−82.7	—	dBm/core
	54 Mbps OFDM	—	−81.2	—	dBm/core
SISO RX sensitivity IEEE 802.11n (10% PER for 4096 octet PSDU) <sup>a</sup> Defined for default parameters: GF, 800 ns GI, and non-STBC.	20 MHz channel spacing for all MCS rates				
	MCS0	—	−95	—	dBm
	MCS1	—	−93.2	—	dBm
	MCS2	—	−90.8	—	dBm
	MCS3	—	−87.2	—	dBm
	MCS4	—	−83.9	—	dBm
	MCS5	—	−79.4	—	dBm
	MCS6	—	−78	—	dBm
	MCS7	—	−76.3	—	dBm

**Table 28: WLAN 2.4 GHz Receiver Performance Specifications (Continued)**

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
MIMO RX sensitivity IEEE 802.11n (10% PER for 4096 octet PSDU) <sup>a</sup> Defined for default parameters: GF, 800 ns GI, and non-STBC.	20 MHz channel spacing for all MCS rates				
	MCS0	—	−97	—	dBm/core
	MCS1	—	−95.2	—	dBm/core
	MCS2	—	−92.8	—	dBm/core
	MCS3	—	−89.2	—	dBm/core
	MCS4	—	−86.9	—	dBm/core
	MCS5	—	−82.4	—	dBm/core
	MCS6	—	−81	—	dBm/core
	MCS7	—	−79.3	—	dBm/core
	MCS8	—	−95.1	—	dBm/core
	MCS15	—	−76.3	—	dBm/core
SISO RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU) <sup>a</sup> Defined for default parameters: GF, 800 ns GI, and non-STBC	20 MHz channel spacing for all MCS rates				
	MCS0, Nss 1	—	−95	—	dBm
	MCS1, Nss 1	—	−92.8	—	dBm
	MCS2, Nss 1	—	−90.5	—	dBm
	MCS3, Nss 1	—	−87	—	dBm
	MCS4, Nss 1	—	−83.9	—	dBm
	MCS5, Nss 1	—	−79.3	—	dBm
	MCS6, Nss 1	—	−77.9	—	dBm
	MCS7, Nss 1	—	−76.1	—	dBm
MIMO RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU) <sup>a</sup> Defined for default parameters: GF, 800 ns GI, and non-STBC	20 MHz channel spacing for all MCS rates				
	MCS0, Nss 1	—	−97	—	dBm/core
	MCS1, Nss 1	—	−94.8	—	dBm/core
	MCS2, Nss 1	—	−92.5	—	dBm/core
	MCS3, Nss 1	—	−89	—	dBm/core
	MCS4, Nss 1	—	−86.9	—	dBm/core
	MCS5, Nss 1	—	−82.3	—	dBm/core
	MCS6, Nss 1	—	−80.9	—	dBm/core
	MCS7, Nss 1	—	−79.1	—	dBm/core
	MCS8, Nss 1	—	−74.9	—	dBm/core
	MCS0, Nss 2	—	−95	—	dBm/core
	MCS8, Nss 2	—	−93	—	dBm/core
SISO RX sensitivity IEEE 802.11ac 20 MHz channel spacing with LDPC (10% PER for 4096 octet PSDU). <sup>a</sup> Defined for default parameters: GF, 800 ns GI, LDPC coding, and non-STBC.	MCS7, Nss 1	—	−78.8	—	dBm
	MCS8, Nss 1	—	−74.8	—	dBm
	MCS9, Nss 1	—	−72.8	—	dBm
MIMO RX sensitivity IEEE 802.11ac 20 MHz channel spacing with LDPC (10% PER for 4096 octet PSDU) <sup>a</sup> . Defined for default parameters: GF, 800 ns GI, LDPC coding, and non-STBC.	MCS7, Nss 1	—	−81.8	—	dBm/core
	MCS8, Nss 1	—	−77.8	—	dBm/core
	MCS9, Nss 1	—	−75.8	—	dBm/core
	MCS7, Nss 2	—	−78.8	—	dBm/core
	MCS8, Nss 2	—	−74.8	—	dBm/core
	MCS9, Nss 2	—	−72.8	—	dBm/core

**Table 28: WLAN 2.4 GHz Receiver Performance Specifications (Continued)**

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
Full BW mode: SISO RX sensitivity IEEE 802.11ax (10% PER for 4096 octet PSDU) <sup>a</sup> : CP/LTF = 0.8 $\mu$ s + 2 $\times$ LTF, LDPC, non-STBC, and 20 MHz BW	MCS0, Nss 1	—	–95.6	—	dBm
	MCS7, Nss 1	—	–78.3	—	dBm
	MCS8, Nss 1	—	–73.8	—	dBm
	MCS9 Nss 1	—	–71.4	—	dBm
Full BW mode: MIMO RX sensitivity IEEE 802.11ax (10% PER for 4096 octet PSDU) <sup>a</sup> : CP/LTF = 0.8 $\mu$ s + 2 $\times$ LTF, LDPC, non-STBC, and 20 MHz BW	MCS0, Nss 1	—	–97.6	—	dBm/core
	MCS7, Nss 1	—	–81.3	—	dBm/core
	MCS8, Nss 1	—	–76.8	—	dBm/core
	MCS9, Nss 1	—	–74.4	—	dBm/core
	MCS0, Nss 2	—	–95.6	—	dBm/core
	MCS7, Nss 2	—	–78.3	—	dBm/core
	MCS8, Nss 2	—	–73.8	—	dBm/core
	MCS9, Nss 2	—	–71.4	—	dBm/core
26 resource units (RU 26): SISO RX sensitivity IEEE 802.11ax (10% PER for 4096 octet PSDU) <sup>a</sup> : CP/LTF = 0.8 $\mu$ s + 2 $\times$ LTF, LDPC, non-STBC, and 20 MHz BW	MCS0, Nss 1	—	–95.2	—	dBm
	MCS7, Nss 1	—	–76.7	—	dBm
	MCS8, Nss 1	—	–72.3	—	dBm
	MCS9, Nss 1	—	–69.9	—	dBm
26 resource units (RU 26): MIMO RX sensitivity IEEE 802.11ax (10% PER for 4096 octet PSDU) <sup>a</sup> : CP/LTF = 0.8 $\mu$ s + 2 $\times$ LTF, LDPC, non-STBC, and 20 MHz BW	MCS0, Nss 1	—	–96.2	—	dBm/core
	MCS7, Nss 1	—	–79.7	—	dBm/core
	MCS8, Nss 1	—	–75.3	—	dBm/core
	MCS9, Nss 1	—	–72.9	—	dBm/core
	MCS0, Nss 2	—	–95.2	—	dBm/core
	MCS7, Nss 2	—	–76.7	—	dBm/core
	MCS8, Nss 2	—	–72.3	—	dBm/core
	MCS9, Nss 2	—	–69.9	—	dBm/core
52 resource units (RU 52): SISO RX sensitivity IEEE 802.11ax (10% PER for 4096 octet PSDU) <sup>a</sup> : CP/LTF = 0.8 $\mu$ s + 2 $\times$ LTF, LDPC, non-STBC, and 20 MHz BW	MCS0, Nss 1	—	–95.4	—	dBm
	MCS7, Nss 1	—	–77.2	—	dBm
	MCS8, Nss 1	—	–73.3	—	dBm
	MCS9 Nss 1	—	–71.3	—	dBm
52 resource units (RU 52): MIMO RX sensitivity IEEE 802.11ax (10% PER for 4096 octet PSDU) <sup>a</sup> : CP/LTF = 0.8 $\mu$ s + 2 $\times$ LTF, LDPC, non-STBC, and 20 MHz BW	MCS0, Nss 1	—	–96.4	—	dBm/core
	MCS7, Nss 1	—	–80.2	—	dBm/core
	MCS8, Nss 1	—	–76.3	—	dBm/core
	MCS9, Nss 1	—	–74.3	—	dBm/core
	MCS0, Nss 2	—	–95.4	—	dBm/core
	MCS7, Nss 2	—	–77.2	—	dBm/core
	MCS8, Nss 2	—	–73.3	—	dBm/core
	MCS9, Nss 2	—	–71.3	—	dBm/core
106 resource units (RU 106): SISO RX sensitivity IEEE 802.11ax (10% PER for 4096 octet PSDU) <sup>a</sup> : CP/LTF = 0.8 $\mu$ s + 2 $\times$ LTF, LDPC, non-STBC, and 20 MHz BW	MCS0, Nss 1	—	–95.5	—	dBm
	MCS7, Nss 1	—	–77.3	—	dBm
	MCS8, Nss 1	—	–73.6	—	dBm
	MCS9 Nss 1	—	–71.3	—	dBm

**Table 28: WLAN 2.4 GHz Receiver Performance Specifications (Continued)**

Parameter	Condition/Notes		Min.	Typ.	Max.	Unit
106 resource units (RU 106): MIMO RX sensitivity IEEE 802.11ax (10% PER for 4096 octet PSDU) <sup>a</sup> : CP/LTF = 0.8 μs + 2 × LTF, LDPC, non-STBC, and 20 MHz BW	MCS0, Nss 1		—	−96.5	—	dBm/core
	MCS7, Nss 1		—	−80.3	—	dBm/core
	MCS8, Nss 1		—	−76.6	—	dBm/core
	MCS9, Nss 1		—	−74.3	—	dBm/core
	MCS0, Nss 2		—	−95.5	—	dBm/core
	MCS7, Nss 2		—	−77.3	—	dBm/core
	MCS8, Nss 2		—	−73.6	—	dBm/core
	MCS9, Nss 2		—	−71.3	—	dBm/core
Range Extension: SISO RX sensitivity IEEE 802.11ax (10% PER for 4096 PSDU) <sup>a</sup> : CP/LTF = 0.8 μs +2 × LTF	MCS0, Nss1 (242 RU)		—	N/A	—	dBm
	MCS1, Nss1 (242 RU)		—	N/A	—	dBm
	MCS2, Nss1 (242 RU)		—	N/A	—	dBm
	MCS0, Nss1 (106 RU)		—	N/A	—	dBm
Range Extension: MIMO RX sensitivity IEEE 802.11ax (10% PER for 4096 PSDU) <sup>a</sup> : CP/LTF = 0.8 μs +2 × LTF	MCS0, Nss1 (242 RU)		—	N/A	—	dBm/core
	MCS1, Nss1 (242 RU)		—	N/A	—	dBm/core
	MCS2, Nss1 (242 RU)		—	N/A	—	dBm/core
	MCS0, Nss1 (106 RU)		—	N/A	—	dBm/core
Blocking level for 12 dB receive sensitivity degradation at the chip input port (without external filtering) <sup>b</sup>	776–794 MHz	CDMA2000	—	−7.3	—	dBm
	824–849 MHz <sup>c</sup>	cdmaOne	—	−7.7	—	dBm
	824–849 MHz <sup>c</sup>	GSM850	—	−10.1	—	dBm
	880–915 MHz	E–GSM	—	−5.7	—	dBm
	1710–1785 MHz	GSM1800	—	−9.5	—	dBm
	1850–1910 MHz	GSM1800	—	−7.9	—	dBm
	1850–1910 MHz	cdmaOne	—	−21.4	—	dBm
	1850–1910 MHz	WCDMA	—	−15.5	—	dBm
	1920–1980 MHz	WCDMA	—	−17.8	—	dBm
	2500–2570 MHz	Band 7	—	−21.7	—	dBm
	2300–2400 MHz	Band 40	—	−24.5	—	dBm
	2570-2620 MHz	Band 38	—	−21.3	—	dBm
	2545-2575 MHz	XGP band	—	−17.2	—	dBm
In-band static CW jammer immunity (fc - 8 MHz < fcw < + 8 MHz)	RX PER < 1%, 54 Mbps OFDM, 1000 octet PSDU for: (RxSense + 23 dB < Rxlevel < max. input level)		−80	—	—	dBm
Input in–band IP3	Maximum LNA gain		—	−12	—	dBm
	Minimum LNA gain		—	7	—	dBm
Maximum receive level @ 2.4 GHz	@ 1, 2 Mbps (8% PER, 1024 octets)		−3.5	—	—	dBm
	@ 5.5, 11 Mbps (8% PER, 1024 octets)		−9.5	—	—	dBm
	@ 6–54 Mbps (10% PER, 1024 octets)		−9.5	—	—	dBm
	@ MCS0–7 rates (10% PER, 4095 octets)		−9.5	—	—	dBm
	@ MCS8–9 rates (10% PER, 4095 octets)		−11	—	—	dBm

**Table 28: WLAN 2.4 GHz Receiver Performance Specifications (Continued)**

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
LPF 3 dB bandwidth	—	—	9	—	MHz
Adjacent channel rejection–DSSS (Difference between interfering and desired signal at 8% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes)	Desired and interfering signal 30 MHz apart				
	1 Mbps DSSS	–74 dBm	35	—	dB
	2 Mbps DSSS	–74 dBm	35	—	dB
	Desired and interfering signal 25 MHz apart				
	5.5 Mbps DSSS	70 dBm	35	—	dB
Adjacent channel rejection OFDM (difference between interfering and desired signal (25 MHz apart) at 10% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes)	11 Mbps DSSS	70 dBm	35	—	dB
	6 Mbps OFDM	79 dBm	16	—	dB
	9 Mbps OFDM	78 dBm	15	—	dB
	12 Mbps OFDM	76 dBm	13	—	dB
	18 Mbps OFDM	74 dBm	11	—	dB
	24 Mbps OFDM	71 dBm	8	—	dB
	36 Mbps OFDM	67 dBm	4	—	dB
	48 Mbps OFDM	63 dBm	0	—	dB
Adjacent channel rejection MCS0–7 IEEE 802.11n (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 4096 octet PSDU with desired signal level as specified in Condition/Notes)	54 Mbps OFDM	62 dBm	–1	—	dB
	MCS0	79 dBm	16	—	dB
	MCS1	76 dBm	15	—	dB
	MCS2	74 dBm	13	—	dB
	MCS3	71 dBm	11	—	dB
	MCS4	67 dBm	8	—	dB
	MCS5	63 dBm	4	—	dB
	MCS6	62 dBm	0	—	dB
Adjacent channel rejection MCS0–9 IEEE 802.11ac (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 4096 octet PSDU with desired signal level as specified in Condition/Notes)	MCS7	61 dBm	–1	—	dB
	MCS0	82 dBm	16	—	dB
	MCS1	80 dBm	15	—	dB
	MCS2	77 dBm	13	—	dB
	MCS3	74 dBm	11	—	dB
	MCS4	70 dBm	8	—	dB
	MCS5	66 dBm	4	—	dB
	MCS6	65 dBm	0	—	dB
	MCS7	64 dBm	–1	—	dB
	MCS8	59 dBm	–2	—	dB
Adjacent channel rejection MCS0–9 IEEE 802.11ax (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 4096 octet PSDU with desired signal level as specified in Condition/Notes)	MCS9	57 dBm	–4	—	dB
	MCS0	82 dBm	16	—	dB
	MCS1	80 dBm	15	—	dB
	MCS2	77 dBm	13	—	dB
	MCS3	74 dBm	11	—	dB
	MCS4	70 dBm	8	—	dB
	MCS5	66 dBm	4	—	dB
	MCS6	65 dBm	0	—	dB
	MCS7	64 dBm	–1	—	dB
	MCS8	59 dBm	–2	—	dB
	MCS9	57 dBm	–4	—	dB

**Table 28: WLAN 2.4 GHz Receiver Performance Specifications (Continued)**

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
Maximum receiver gain	—	—	62	—	dB
Gain control step	—	—	3	—	dB
RSSI accuracy <sup>d</sup>	Range 90 dBm to 30 dBm	-2	—	2	dB
	Range above 30 dBm	-2	—	2	dB
Return loss	Z <sub>o</sub> = 50Ω, across the dynamic range	10	—	13	dB
Receiver cascaded noise figure	At maximum gain	—	4	—	dB

- a. Sensitivity degradations for alternate settings in MCS modes. MM: 0.5 dB drop, and SGI: 2 dB drop.
- b. The cellular standard listed for each band shows the modulation type to generate an interfering signal in that band for purpose of this test. It is not intended to indicate any specific usage of each band in any specific country.
- c. The blocking levels are valid for channels 1 to 11. (For higher channels, the performance may be lower due to third harmonic signals (3 × 824 MHz) falling within band.)
- d. The minimum and maximum values shown have a 95% confidence level.

## 8.4 WLAN 2.4 GHz Transmitter Performance Specifications

**NOTE:** The values shown in Table 29 are specified at the RF port unless otherwise noted.

**Table 29: WLAN 2.4 GHz Transmitter Performance Specifications**

Parameter	Condition/Notes		Min.	Typ.	Max.	Unit
Frequency range	—		2400	—	2500	MHz
Transmitted power in cellular and FM bands (at 18 dBm, 100% duty cycle, 1 Mbps CCK) <sup>a</sup>	76–108 MHz	FM RX	—	N/A	—	dBm/Hz
	776–794 MHz		—	–163.5	—	dBm/Hz
	869–960 MHz	cdmaOne, GSM850	—	–161.2	—	dBm/Hz
	925–960 MHz	E-GSM	—	–161.2	—	dBm/Hz
	1570–1580 MHz	GPS	—	–146.1	—	dBm/Hz
	1805–1880 MHz	GSM1800	—	–138.9	—	dBm/Hz
	1930–1990 MHz	GSM1900, cdmaOne, WCDMA	—	–133.2	—	dBm/Hz
	2110–2170 MHz	WCDMA	—	–127.3	—	dBm/Hz
	2500–2570 MHz	Band 7	—	–102	—	dBm/Hz
	2300–2400 MHz	Band 40	—	–83.6	—	dBm/Hz
	2570–2620 MHz	Band 38	—	–118.2	—	dBm/Hz
	2545–2575 MHz	XGP Band	—	–116	—	dBm/Hz
Harmonic level (at 18 dBm with 100% duty cycle)	4.8–5.0 GHz	2 <sup>nd</sup> harmonic	—	–33	—	dBm/1 MHz
	7.2–7.5 GHz	3 <sup>rd</sup> harmonic	—	–60.8	—	dBm/1 MHz
TX power at RF port for highest power level setting at 25°C with spectral mask and EVM compliance		<b>EVM Does Not Exceed</b>				
	802.11b (DSSS/CCK)	–9 dB	20	21	—	dBm
	OFDM, BPSK	–8 dB	19	20	—	dBm
	OFDM, QPSK	–13 dB	19	20	—	dBm
	OFDM, 16-QAM	–19 dB	19	20	—	dBm
	OFDM, 64-QAM (R = 3/4)	–25 dB	19	20	—	dBm
	OFDM, 64-QAM (R = 5/6)	–27 dB	19	20	—	dBm
	OFDM, 256-QAM (R = 3/4, VHT20)	–30 dB	17	18	—	dBm
	OFDM, 256-QAM (R = 5/6, VHT20)	–32 dB	16	17	—	dBm
TX power control dynamic range	—		—	30	—	dB
Closed-loop TX power variation <sup>b</sup>	Over the full temperature and voltage ranges		—	—	±1.5	dB
Carrier suppression	—		15	32	—	dBc
Gain control step	—		—	0.5	—	dB
Return loss at chip port TX	Zo = 50Ω		TBD	TBD	—	dB

a. The cellular standards listed only indicate the typical usages of that band in some countries; other standards may also be used within those bands.

b. Applies to an 8 dBm to 20 dBm TX power output range with production PA trimming. Applies to a –10 dBm to 20 dBm TX power output range with PA trimming and open-loop power control (OLPC) calibration in production.

## 8.5 WLAN 5 GHz Receiver Performance Specifications

**NOTE:** The values shown in [Table 30](#) are specified at the RF port unless otherwise noted.

**Table 30: WLAN 5 GHz Receiver Performance Specifications**

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
Frequency range	—	4900	—	5845	MHz
SISO RX sensitivity IEEE 802.11g (10% PER for 1000 octet PSDU)	6 Mbps OFDM	—	−95	—	dBm
	9 Mbps OFDM	—	−93.5	—	dBm
	12 Mbps OFDM	—	−92.3	—	dBm
	18 Mbps OFDM	—	−89.9	—	dBm
	24 Mbps OFDM	—	−86.9	—	dBm
	36 Mbps OFDM	—	−83.4	—	dBm
	48 Mbps OFDM	—	−79	—	dBm
	54 Mbps OFDM	—	−77.5	—	dBm
MIMO RX sensitivity IEEE 802.11g (10% PER for 1024 octet PSDU) <sup>a</sup>	6 Mbps OFDM	—	−97	—	dBm/core
	9 Mbps OFDM	—	−95.5	—	dBm/core
	12 Mbps OFDM	—	−94.3	—	dBm/core
	18 Mbps OFDM	—	−92.9	—	dBm/core
	24 Mbps OFDM	—	−89.9	—	dBm/core
	36 Mbps OFDM	—	−86.4	—	dBm/core
	48 Mbps OFDM	—	−82	—	dBm/core
	54 Mbps OFDM	—	−80.5	—	dBm/core
SISO RX sensitivity IEEE 802.11n (10% PER for 4096 octet PSDU) <sup>a</sup> Defined for default parameters: GF, 800 ns GI, and non-STBC.	20 MHz channel spacing for all MCS rates				
	MCS0	—	−94.8	—	dBm
	MCS1	—	−92.3	—	dBm
	MCS2	—	−90	—	dBm
	MCS3	—	−86.4	—	dBm
	MCS4	—	−83.2	—	dBm
	MCS5	—	−78.8	—	dBm
	MCS6	—	−77.2	—	dBm
MIMO RX sensitivity IEEE 802.11n (10% PER for 4096 octet PSDU) <sup>a</sup> Defined for default parameters: GF, 800 ns GI, and non-STBC.	20 MHz channel spacing for all MCS rates				
	MCS0	—	−96.8	—	dBm/core
	MCS1	—	−94.3	—	dBm/core
	MCS2	—	−92	—	dBm/core
	MCS3	—	−89.4	—	dBm/core
	MCS4	—	−86.2	—	dBm/core
	MCS5	—	−81.8	—	dBm/core
	MCS6	—	−80.2	—	dBm/core
	MCS7	—	−78.5	—	dBm/core
	MCS8	—	−94.8	—	dBm/core
	MCS15	—	−75.5	—	dBm/core

**Table 30: WLAN 5 GHz Receiver Performance Specifications (Continued)**

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
SISO RX sensitivity IEEE 802.11n (10% PER for 4096 octet PSDU) <sup>a</sup> Defined for default parameters: GF, 800 ns GI, and non-STBC.	40 MHz channel spacing for all MCS rates				
	MCS0	—	–92.4	—	dBm
	MCS1	—	–89.8	—	dBm
	MCS2	—	–87.2	—	dBm
	MCS3	—	–83.6	—	dBm
	MCS4	—	–80.3	—	dBm
	MCS5	—	–76.1	—	dBm
	MCS6	—	–74.4	—	dBm
MIMO RX sensitivity IEEE 802.11n (10% PER for 4096 octet PSDU) <sup>a</sup> Defined for default parameters: GF, 800 ns GI, and non-STBC.	40 MHz channel spacing for all MCS rates				
	MCS0	—	–94.4	—	dBm/core
	MCS1	—	–91.8	—	dBm/core
	MCS2	—	–89.2	—	dBm/core
	MCS3	—	–86.6	—	dBm/core
	MCS4	—	–83.3	—	dBm/core
	MCS5	—	–79.1	—	dBm/core
	MCS6	—	–77.4	—	dBm/core
	MCS7	—	–75.7	—	dBm/core
	MCS8	—	–92.4	—	dBm/core
	MCS15	—	–72.7	—	dBm/core
SISO RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU) <sup>a</sup> Defined for default parameters: GF, 800 ns GI, and non-STBC	20 MHz channel spacing for all MCS rates				
	MCS0, Nss 1	—	–94.8	—	dBm
	MCS1, Nss 1	—	–92.3	—	dBm
	MCS2, Nss 1	—	–90	—	dBm
	MCS3, Nss 1	—	–86.4	—	dBm
	MCS4, Nss 1	—	–83.2	—	dBm
	MCS5, Nss 1	—	–78.8	—	dBm
	MCS6, Nss 1	—	–77.2	—	dBm
	MCS7, Nss 1	—	–75.5	—	dBm
MIMO RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU) <sup>a</sup> Defined for default parameters: GF, 800 ns GI, and non-STBC	20 MHz channel spacing for all MCS rates				
	MCS0, Nss 1	—	–96.8	—	dBm/core
	MCS1, Nss 1	—	–94.3	—	dBm/core
	MCS2, Nss 1	—	–92	—	dBm/core
	MCS3, Nss 1	—	–89.4	—	dBm/core
	MCS4, Nss 1	—	–86.2	—	dBm/core
	MCS5, Nss 1	—	–81.8	—	dBm/core
	MCS6, Nss 1	—	–80.2	—	dBm/core
	MCS7, Nss 1	—	–78.5	—	dBm/core
	MCS8, Nss 1	—	–74.5	—	dBm/core
	MCS9, Nss 1	—	–74.9	—	dBm/core
	MCS0, Nss 2	—	–94.8	—	dBm/core
	MCS8, Nss 2	—	–71.4	—	dBm/core
	MCS9, Nss 2	—	–72.1	—	dBm/core

**Table 30: WLAN 5 GHz Receiver Performance Specifications (Continued)**

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
SISO RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU) <sup>a</sup> Defined for default parameters: GF, 800 ns GI, and non-STBC.	40 MHz channel spacing for all MCS rates				
	MCS0, Nss 1	—	–92.2	—	dBm
	MCS1, Nss 1	—	–89.7	—	dBm
	MCS2, Nss 1	—	–87.2	—	dBm
	MCS3, Nss 1	—	–83.5	—	dBm
	MCS4, Nss 1	—	–80.3	—	dBm
	MCS5, Nss 1	—	–76	—	dBm
	MCS6, Nss 1	—	–74.4	—	dBm
MIMO RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU) <sup>a</sup> Defined for default parameters: GF, 800 ns GI, and non-STBC.	40 MHz channel spacing for all MCS rates				
	MCS0, Nss 1	—	–94.2	—	dBm/core
	MCS1, Nss 1	—	–91.7	—	dBm/core
	MCS2, Nss 1	—	–89.2	—	dBm/core
	MCS3, Nss 1	—	–86.5	—	dBm/core
	MCS4, Nss 1	—	–83.3	—	dBm/core
	MCS5, Nss 1	—	–79	—	dBm/core
	MCS6, Nss 1	—	–77.4	—	dBm/core
	MCS7, Nss 1	—	–75.4	—	dBm/core
	MCS8, Nss 1	—	–71.6	—	dBm/core
	MCS9, Nss 1	—	–69.8	—	dBm/core
	MCS0, Nss 2	—	–92.2	—	dBm/core
	MCS8, Nss 2	—	–66.8	—	dBm/core
	MCS9, Nss 2	—	–68.5	—	dBm/core
SISO RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU) <sup>a</sup> Defined for default parameters: GF, 800 ns GI, and non-STBC.	80 MHz channel spacing for all MCS rates				
	MCS0, Nss 1	—	–89.2	—	dBm
	MCS1, Nss 1	—	–86.7	—	dBm
	MCS2, Nss 1	—	–84.1	—	dBm
	MCS3, Nss 1	—	–80.4	—	dBm
	MCS4, Nss 1	—	–77.2	—	dBm
	MCS5, Nss 1	—	–73	—	dBm
	MCS6, Nss 1	—	–71.4	—	dBm
	MCS7, Nss 1	—	–69.9	—	dBm

**Table 30: WLAN 5 GHz Receiver Performance Specifications (Continued)**

Parameter	Condition/Notes		Min.	Typ.	Max.	Unit
MIMO RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU) <sup>a</sup> Defined for default parameters: GF, 800 ns GI, and non-STBC.	80 MHz channel spacing for all MCS rates					
	MCS0, Nss 1		—	–91.2	—	dBm/core
	MCS1, Nss 1		—	–88.7	—	dBm/core
	MCS2, Nss 1		—	–86.1	—	dBm/core
	MCS3, Nss 1		—	–83.4	—	dBm/core
	MCS4, Nss 1		—	–80.2	—	dBm/core
	MCS5, Nss 1		—	–76	—	dBm/core
	MCS6, Nss 1		—	–74.4	—	dBm/core
	MCS7, Nss 1		—	–72.9	—	dBm/core
	MCS8, Nss 1		—	–68.7	—	dBm/core
	MCS9, Nss 1		—	–67.1	—	dBm/core
	MCS0, Nss 2		—	–89.2	—	dBm/core
	MCS8, Nss 2		—	–69.9	—	dBm/core
	MCS9, Nss 2		—	–65.7	—	dBm/core
SISO RX sensitivity IEEE 802.11ac 20/40/80 MHz channel spacing with LDPC (10% PER for 4096 octet PSDU) <sup>a</sup> at WLAN RF port. Defined for default parameters: GF, 800 ns GI, LDPC coding, and non-STBC.	MCS7, Nss 1	20 MHz	—	–78.9	—	dBm
	MCS8, Nss 1	20 MHz	—	–75.1	—	dBm
	MCS9, Nss 1	20 MHz	—	–71.2	—	dBm
	MCS7, Nss 1	40 MHz	—	–76	—	dBm
	MCS8, Nss 1	40 MHz	—	–72.2	—	dBm
	MCS9, Nss 1	40 MHz	—	–70.2	—	dBm
	MCS7, Nss 1	80 MHz	—	–73.2	—	dBm
	MCS8, Nss 1	80 MHz	—	–69.5	—	dBm
	MCS9, Nss 1	80 MHz	—	–67.4	—	dBm
MIMO RX sensitivity IEEE 802.11ac 20/40/80 MHz channel spacing with LDPC (10% PER for 4096 octet PSDU) <sup>a</sup> at WLAN RF port. Defined for default parameters: GF, 800 ns GI, LDPC coding, and non-STBC.	MCS7, Nss 2	20 MHz	—	–79	—	dBm/core
	MCS8, Nss 2	20 MHz	—	–75.2	—	dBm/core
	MCS9, Nss 2	20 MHz	—	–75.2	—	dBm/core
	MCS7, Nss 2	40 MHz	—	–76.1	—	dBm/core
	MCS8, Nss 2	40 MHz	—	–72.3	—	dBm/core
	MCS9, Nss 2	40 MHz	—	–70.3	—	dBm/core
	MCS7, Nss 2	80 MHz	—	–73.1	—	dBm/core
	MCS8, Nss 2	80 MHz	—	–69.6	—	dBm/core
	MCS9, Nss 2	80 MHz	—	–67.6	—	dBm/core
Range Extension: SISO RX sensitivity IEEE 802.11ax (10% PER for 4096 PSDU) <sup>a</sup> : CP/LTF = 0.8 $\mu$ s + 2 $\times$ LTF	MCS0, Nss1	242 RU	—	TBD	—	dBm
	MCS1, Nss1	242 RU	—	TBD	—	dBm
	MCS2, Nss1	242 RU	—	TBD	—	dBm
	MCS0, Nss1	106 RU	—	TBD	—	dBm
Range Extension MIMO RX sensitivity IEEE 802.11ax (10% PER for 4096 PSDU) <sup>a</sup> : CP/LTF = 0.8 $\mu$ s + 2 $\times$ LTF	MCS0, Nss1	242 RU	—	TBD	—	dBm/core
	MCS1, Nss1	242 RU	—	TBD	—	dBm/core
	MCS2, Nss1	242 RU	—	TBD	—	dBm/core
	MCS0, Nss1	106 RU	—	TBD	—	dBm/core

**Table 30: WLAN 5 GHz Receiver Performance Specifications (Continued)**

Parameter	Condition/Notes		Min.	Typ.	Max.	Unit
Full BW mode: SISO RX sensitivity IEEE 802.11ax (10% PER for 4096 octet PSDU) <sup>a</sup> : CP/LTF = 0.8 $\mu$ s + 2 $\times$ LTF, LDPC, non-STBC, and 20/40/80 MHz BW	MCS0, Nss 1	20 MHz	—	–95.3	—	dBm
	MCS7, Nss 1	20 MHz	—	–78.1	—	dBm
	MCS8, Nss 1	20 MHz	—	–73.2	—	dBm
	MCS9, Nss 1	20 MHz	—	–71.3	—	dBm
	MCS10, Nss 1	20 MHz	—	–67	—	dBm
	MCS11, Nss 1	20 MHz	—	–63.8	—	dBm
	MCS0, Nss 1	40 MHz	—	–93	—	dBm
	MCS7, Nss 1	40 MHz	—	–75.3	—	dBm
	MCS8, Nss 1	40 MHz	—	–71	—	dBm
	MCS9, Nss 1	40 MHz	—	–69.2	—	dBm
	MCS10, Nss 1	40 MHz	—	–65	—	dBm
	MCS11, Nss 1	40 MHz	—	–61.7	—	dBm
	MCS0, Nss 1	80 MHz	—	–89.8	—	dBm
	MCS7, Nss 1	80 MHz	—	–72.3	—	dBm
	MCS8, Nss 1	80 MHz	—	–67.2	—	dBm
	MCS9, Nss 1	80 MHz	—	–66	—	dBm
	MCS10, Nss 1	80 MHz	—	–61.5	—	dBm
	MCS11, Nss 1	80 MHz	—	–58.3	—	dBm
Full BW mode: MIMO RX sensitivity IEEE 802.11ax (10% PER for 4096 octet PSDU) <sup>a</sup> : CP/LTF = 0.8 $\mu$ s + 2 $\times$ LTF, LDPC, non-STBC, and 20/40/80 MHz BW	MCS0, Nss 2	20 MHz	—	–95.3	—	dBm
	MCS7, Nss 2	20 MHz	—	–78.1	—	dBm
	MCS8, Nss 2	20 MHz	—	–73.2	—	dBm
	MCS9, Nss 2	20 MHz	—	–71.3	—	dBm
	MCS10, Nss 2	20 MHz	—	–67	—	dBm
	MCS11, Nss 2	20 MHz	—	–63.8	—	dBm
	MCS0, Nss 2	40 MHz	—	–93	—	dBm
	MCS7, Nss 2	40 MHz	—	–75.3	—	dBm
	MCS8, Nss 2	40 MHz	—	–71	—	dBm
	MCS9, Nss 2	40 MHz	—	–69.2	—	dBm
	MCS10, Nss 2	40 MHz	—	–65	—	dBm
	MCS11, Nss 2	40 MHz	—	–61.7	—	dBm
	MCS0, Nss 2	80 MHz	—	–89.8	—	dBm
	MCS7, Nss 2	80 MHz	—	–72.3	—	dBm
	MCS8, Nss 2	80 MHz	—	–67.2	—	dBm
	MCS9, Nss 2	80 MHz	—	–66	—	dBm
	MCS10, Nss 2	80 MHz	—	–61.5	—	dBm
	MCS11, Nss 2	80 MHz	—	–58.3	—	dBm

**Table 30: WLAN 5 GHz Receiver Performance Specifications (Continued)**

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
26 resource units (RU 26): SISO RX sensitivity IEEE 802.11ax (10% PER for 4096 octet PSDU) <sup>a</sup> : CP/LTF = 0.8 $\mu$ s + 2 $\times$ LTF, LDPC, non-STBC, and 20 MHz BW	MCS0, Nss 1	—	–95	—	dBm
	MCS7, Nss 1	—	–76.3	—	dBm
	MCS8, Nss 1	—	–72.2	—	dBm
	MCS9 Nss 1	—	–70.1	—	dBm
	MCS10, Nss 1	—	N/A	—	dBm
	MCS11, Nss 1	—	N/A	—	dBm
26 resource units (RU 26): MIMO RX sensitivity IEEE 802.11ax (10% PER for 4096 octet PSDU) <sup>a</sup> : CP/LTF = 0.8 $\mu$ s + 2 $\times$ LTF, LDPC, non-STBC, and 20 MHz BW	MCS0, Nss 1	—	–97	—	dBm/core
	MCS7, Nss 1	—	–79.3	—	dBm/core
	MCS8, Nss 1	—	–75.2	—	dBm/core
	MCS9, Nss 1	—	–73.1	—	dBm/core
	MCS10, Nss 1	—	N/A	—	dBm/core
	MCS11, Nss 1	—	N/A	—	dBm/core
	MCS0, Nss 2	—	–95	—	dBm/core
	MCS7, Nss 2	—	–76.3	—	dBm/core
	MCS8, Nss 2	—	–72.2	—	dBm/core
	MCS9, Nss 2	—	–70.1	—	dBm/core
	MCS10, Nss 2	—	N/A	—	dBm/core
	MCS11, Nss 2	—	N/A	—	dBm/core
52 resource units (RU 52): SISO RX sensitivity IEEE 802.11ax (10% PER for 4096 octet PSDU) <sup>a</sup> : CP/LTF = 0.8 $\mu$ s + 2 $\times$ LTF, LDPC, non-STBC, and 20 MHz BW	MCS0, Nss 1	—	–95.3	—	dBm
	MCS7, Nss 1	—	–76.7	—	dBm
	MCS8, Nss 1	—	–73	—	dBm
	MCS9 Nss 1	—	–70.9	—	dBm
	MCS10, Nss 1	—	N/A	—	dBm
	MCS11, Nss 1	—	N/A	—	dBm
52 resource units (RU 52): MIMO RX sensitivity IEEE 802.11ax (10% PER for 4096 octet PSDU) <sup>a</sup> : CP/LTF = 0.8 $\mu$ s + 2 $\times$ LTF, LDPC, non-STBC, and 20 MHz BW	MCS0, Nss 1	—	–97.3	—	dBm/core
	MCS7, Nss 1	—	–79.7	—	dBm/core
	MCS8, Nss 1	—	–76	—	dBm/core
	MCS9, Nss 1	—	–73.9	—	dBm/core
	MCS10, Nss 1	—	N/A	—	dBm/core
	MCS11, Nss 1	—	N/A	—	dBm/core
	MCS0, Nss 2	—	–95.3	—	dBm/core
	MCS7, Nss 2	—	–76.7	—	dBm/core
	MCS8, Nss 2	—	–73	—	dBm/core
	MCS9, Nss 2	—	–70.9	—	dBm/core
	MCS10, Nss 2	—	N/A	—	dBm/core
	MCS11, Nss 2	—	N/A	—	dBm/core

**Table 30: WLAN 5 GHz Receiver Performance Specifications (Continued)**

Parameter	Condition/Notes		Min.	Typ.	Max.	Unit
106 resource units (RU 106): SISO RX sensitivity IEEE 802.11ax (10% PER for 4096 octet PSDU) <sup>a</sup> : CP/LTF = 0.8 $\mu$ s + 2 $\times$ LTF, LDPC, non-STBC, and 20 MHz BW	MCS0, Nss 1		—	–95.4	—	dBm
	MCS7, Nss 1		—	–77.1	—	dBm
	MCS8, Nss 1		—	–72.7	—	dBm
	MCS9, Nss 1		—	–71.1	—	dBm
	MCS10, Nss 1		—	N/A	—	dBm
	MCS11, Nss 1		—	N/A	—	dBm
106 resource units (RU 106): MIMO RX sensitivity IEEE 802.11ax (10% PER for 4096 octet PSDU) <sup>a</sup> : CP/LTF = 0.8 $\mu$ s + 2 $\times$ LTF, LDPC, non-STBC, and 20 MHz BW	MCS0, Nss 1		—	–97.4	—	dBm/core
	MCS7, Nss 1		—	–80.1	—	dBm/core
	MCS8, Nss 1		—	–75.7	—	dBm/core
	MCS9, Nss 1		—	–74.1	—	dBm/core
	MCS10, Nss 1		—	N/A	—	dBm/core
	MCS11, Nss 1		—	N/A	—	dBm/core
	MCS0, Nss 2		—	–95.4	—	dBm/core
	MCS7, Nss 2		—	–77.1	—	dBm/core
	MCS8, Nss 2		—	–72.7	—	dBm/core
	MCS9, Nss 2		—	–71.1	—	dBm/core
	MCS10, Nss 2		—	N/A	—	dBm/core
	MCS11, Nss 2		—	N/A	—	dBm/core
	MCS0, Nss 1	40 MHz	—	–92.9	—	dBm
	MCS7, Nss 1	40 MHz	—	–75	—	dBm
242 resource units (RU 242): SISO RX sensitivity IEEE 802.11ax (10% PER for 4096 octet PSDU) <sup>a</sup> : CP/LTF = 0.8 $\mu$ s + 2 $\times$ LTF, LDPC, non-STBC, and 40/80 MHz BW	MCS8, Nss 1	40 MHz	—	–69.7	—	dBm
	MCS9, Nss 1	40 MHz	—	–68.2	—	dBm
	MCS10, Nss 1	40 MHz	—	–63.8	—	dBm
	MCS11, Nss 1	40 MHz	—	–60.8	—	dBm
	MCS0, Nss 1	80 MHz	—	–89.7	—	dBm
	MCS7, Nss 1	80 MHz	—	–71.2	—	dBm
	MCS8, Nss 1	80 MHz	—	–66.3	—	dBm
	MCS9, Nss 1	80 MHz	—	–65.1	—	dBm
	MCS10, Nss 1	80 MHz	—	–60.4	—	dBm
	MCS11, Nss 1	80 MHz	—	–56.9	—	dBm

**Table 30: WLAN 5 GHz Receiver Performance Specifications (Continued)**

Parameter	Condition/Notes		Min.	Typ.	Max.	Unit
242 resource units (RU 242): MIMO RX sensitivity IEEE 802.11ax (10% PER for 4096 octet PSDU) <sup>a</sup> : CP/LTF = 0.8 $\mu$ s + 2 $\times$ LTF, LDPC, non-STBC, and 40/80 MHz BW	MCS0, Nss 1	40 MHz	—	–94.9	—	dBm/core
	MCS7, Nss 1	40 MHz	—	–78	—	dBm/core
	MCS8, Nss 1	40 MHz	—	–72.7	—	dBm/core
	MCS9, Nss 1	40 MHz	—	–71.2	—	dBm/core
	MCS10, Nss 1	40 MHz	—	–66.8	—	dBm/core
	MCS11, Nss 1	40 MHz	—	–63.8	—	dBm/core
	MCS0, Nss 1	80 MHz	—	–91.7	—	dBm/core
	MCS7, Nss 1	80 MHz	—	–74.2	—	dBm/core
	MCS8, Nss 1	80 MHz	—	–69.3	—	dBm/core
	MCS9, Nss 1	80 MHz	—	–68.1	—	dBm/core
	MCS10, Nss 1	80 MHz	—	–63.4	—	dBm/core
	MCS11, Nss 1	80 MHz	—	–59.9	—	dBm/core
	MCS0, Nss 2	40 MHz	—	–92.9	—	dBm/core
	MCS7, Nss 2	40 MHz	—	–75	—	dBm/core
	MCS8, Nss 2	40 MHz	—	–69.7	—	dBm/core
	MCS9, Nss 2	40 MHz	—	–68.2	—	dBm/core
	MCS10, Nss 2	40 MHz	—	–63.8	—	dBm/core
	MCS11, Nss 2	40 MHz	—	–60.8	—	dBm/core
	MCS0, Nss 2	80 MHz	—	–89.7	—	dBm/core
	MCS7, Nss 2	80 MHz	—	–71.2	—	dBm/core
	MCS8, Nss 2	80 MHz	—	–66.3	—	dBm/core
	MCS9, Nss 2	80 MHz	—	–65.1	—	dBm/core
	MCS10, Nss 2	80 MHz	—	–60.4	—	dBm/core
	MCS11, Nss 2	80 MHz	—	–56.9	—	dBm/core
484 resource units (RU 484): SISO RX sensitivity IEEE 802.11ax (10% PER for 4096 octet PSDU) <sup>a</sup> : CP/LTF = 0.8 $\mu$ s + 2 $\times$ LTF, LDPC, non-STBC, and 80 MHz BW	MCS0, Nss 1	80 MHz	—	–89.6	—	dBm
	MCS7, Nss 1	80 MHz	—	–71.1	—	dBm
	MCS8, Nss 1	80 MHz	—	–66.3	—	dBm
	MCS9, Nss 1	80 MHz	—	–65.2	—	dBm
	MCS10, Nss 1	80 MHz	—	–60.3	—	dBm
	MCS11, Nss 1	80 MHz	—	–57.8	—	dBm

**Table 30: WLAN 5 GHz Receiver Performance Specifications (Continued)**

Parameter	Condition/Notes		Min.	Typ.	Max.	Unit
484 resource units (RU 484): MIMO RX sensitivity IEEE 802.11ax (10% PER for 4096 octet PSDU) <sup>a</sup> : CP/LTF = 0.8 $\mu$ s + 2 $\times$ LTF, LDPC, non-STBC, and 80 MHz BW	MCS0, Nss 1	80 MHz	—	–91.6	—	dBm/core
	MCS7, Nss 1	80 MHz	—	–74.1	—	dBm/core
	MCS8, Nss 1	80 MHz	—	–69.3	—	dBm/core
	MCS9, Nss 1	80 MHz	—	–68.2	—	dBm/core
	MCS10, Nss 1	80 MHz	—	–63.3	—	dBm/core
	MCS11, Nss 1	80 MHz	—	–60.8	—	dBm/core
	MCS0, Nss 2	80 MHz	—	–89.6	—	dBm/core
	MCS7, Nss 2	80 MHz	—	–71.1	—	dBm/core
	MCS8, Nss 2	80 MHz	—	–66.3	—	dBm/core
	MCS9, Nss 2	80 MHz	—	–65.2	—	dBm/core
	MCS10, Nss 2	80 MHz	—	–60.3	—	dBm/core
	MCS11, Nss 2	80 MHz	—	–57.8	—	dBm/core
Blocking level for 12 dB RX sensitivity degradation at the chip input port (without external filtering) <sup>b</sup>	776–794 MHz	CDMA2000	—	–4.4	—	dBm
	824–849 MHz <sup>c</sup>	cdmaOne	—	–2.2	—	dBm
	824–849 MHz <sup>c</sup>	GSM850	—	–2.2	—	dBm
	880–915 MHz	E-GSM	—	–4.7	—	dBm
	1710–1785 MHz	GSM1800	—	–1.8	—	dBm
	1850–1910 MHz	GSM1800	—	–0.7	—	dBm
	1850–1910 MHz	cdmaOne	—	–0.7	—	dBm
	1850–1910 MHz	WCDMA	—	–0.4	—	dBm
	1920–1980 MHz	WCDMA	—	–2.6	—	dBm
	2500–2570 MHz	Band 7	—	–8.5	—	dBm
	2300–2400 MHz	Band 40	—	–10.6	—	dBm
	2570–2620 MHz	Band 38	—	–8.5	—	dBm
	2545–2575 MHz	XGP Band	—	–8.2	—	dBm
Input in-band IP3	Maximum LNA gain		—	–10	—	dBm
	Minimum LNA gain		—	7	—	dBm
Maximum receive level	@ 6, 9, 12 Mbps		—	–9	—	dBm
	@ 18, 24, 36, 48, 54 Mbps		—	–9	—	dBm
	MCS0 to MCS9	802.11ac	—	–9	—	dBm
LPF 3 dB bandwidth	—		9	—	36	MHz
Adjacent channel rejection – OFDM (Difference between interfering and desired signal (20 MHz apart) at 10% PER for 1000 octet PSDU with desired signal level as specified in Condition/Notes)	6 Mbps OFDM	–79 dBm	16	—	—	dB
	9 Mbps OFDM	–78 dBm	15	—	—	dB
	12 Mbps OFDM	–76 dBm	13	—	—	dB
	18 Mbps OFDM	–74 dBm	11	—	—	dB
	24 Mbps OFDM	–71 dBm	8	—	—	dB
	36 Mbps OFDM	–67 dBm	4	—	—	dB
	48 Mbps OFDM	–63 dBm	0	—	—	dB
	54 Mbps OFDM	–62 dBm	–1	—	—	dB
	65 Mbps OFDM	–61 dBm	–2	—	—	dB

**Table 30: WLAN 5 GHz Receiver Performance Specifications (Continued)**

Parameter	Condition/Notes		Min.	Typ.	Max.	Unit
Adjacent channel rejection – OFDM (Difference between interfering and desired signal (40 MHz apart) at 10% PER for 1000 <sup>d</sup> octet PSDU with desired signal level as specified in Condition/Notes)	6 Mbps OFDM	–78.5 dBm	32	—	—	dB
	9 Mbps OFDM	–77.5 dBm	31	—	—	dB
	12 Mbps OFDM	–75.5 dBm	29	—	—	dB
	18 Mbps OFDM	–73.5 dBm	27	—	—	dB
	24 Mbps OFDM	–70.5 dBm	24	—	—	dB
	36 Mbps OFDM	–66.5 dBm	20	—	—	dB
	48 Mbps OFDM	–62.5 dBm	16	—	—	dB
	54 Mbps OFDM	–61.5 dBm	15	—	—	dB
	65 Mbps OFDM	–60.5 dBm	14	—	—	dB
Adjacent channel rejection MCS0–7 IEEE 802.11n (Difference between interfering and desired signal (20 MHz apart) at 10% PER for 4096 octet PSDU with desired signal level as specified in Condition/Notes)	MCS0	–79 dBm	16	—	—	dB
	MCS1	–76 dBm	13	—	—	dB
	MCS2	–74 dBm	11	—	—	dB
	MCS3	–71 dBm	8	—	—	dB
	MCS4	–67 dBm	4	—	—	dB
	MCS5	–63 dBm	0	—	—	dB
	MCS6	–62 dBm	–1	—	—	dB
	MCS7	–61 dBm	–2	—	—	dB
Adjacent channel rejection MCS0–9 IEEE 802.11ac (Difference between interfering and desired signal (20 MHz apart) at 10% PER for 4096 octet PSDU with desired signal level as specified in Condition/Notes)	MCS0	–82 dBm	16	—	—	dB
	MCS1	–80 dBm	13	—	—	dB
	MCS2	–77 dBm	11	—	—	dB
	MCS3	–74 dBm	8	—	—	dB
	MCS4	–70 dBm	4	—	—	dB
	MCS5	–66 dBm	0	—	—	dB
	MCS6	–65 dBm	–1	—	—	dB
	MCS7	–64 dBm	–2	—	—	dB
	MCS8	–59 dBm	–7	—	—	dB
	MCS9	–57 dBm	–9	—	—	dB
Adjacent channel rejection MCS0–9 IEEE 802.11ax (Difference between interfering and desired signal (20 MHz apart) at 10% PER for 4096 octet PSDU with desired signal level as specified in Condition/Notes)	MCS0	–82 dBm	16	—	—	dB
	MCS1	–80 dBm	13	—	—	dB
	MCS2	–77 dBm	11	—	—	dB
	MCS3	–74 dBm	8	—	—	dB
	MCS4	–70 dBm	4	—	—	dB
	MCS5	–66 dBm	0	—	—	dB
	MCS6	–65 dBm	–1	—	—	dB
	MCS7	–64 dBm	–2	—	—	dB
	MCS8	–59 dBm	–7	—	—	dB
	MCS9	–57 dBm	–9	—	—	dB
	MCS10	–53 dBm	–12	—	—	dB
	MCS11	–50 dBm	–14	—	—	dB
Maximum receiver gain	—		—	62	—	dB

**Table 30: WLAN 5 GHz Receiver Performance Specifications (Continued)**

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
Gain control step	—	—	3	—	dB
RSSI accuracy	Range –90 dBm to –30 dBm	2	—	2	dB
	Range above –30 dBm	2	—	2	dB
Return loss	$Z_0 = 50\Omega$ , across the dynamic range	10	—	13	dB
Receiver cascaded noise figure	At maximum gain	—	4	—	dB

- The cellular standard listed for each band indicates the type of modulation used to generate the interfering signal in that band for the purpose of this test. It is not intended to indicate any specific usage of each band in any specific country.
- The cellular standard listed for each band indicates the type of modulation used to generate the interfering signal in that band for the purpose of this test. It is not intended to indicate any specific usage of each band in any specific country.
- The blocking levels are valid for channels 1 to 11. (For higher channels, the performance may be lower due to third harmonic signals (TBD × TBD MHz) falling within band.)

## 8.6 WLAN 5 GHz Transmitter Performance Specifications

**NOTE:** The values in Table 31 are specified at the RF port unless otherwise noted.

**Table 31: WLAN 5 GHz Transmitter Performance Specifications**

Parameter	Condition/Notes		Min.	Typ.	Max.	Unit
Frequency range	—		4900	—	5845	MHz
Transmitted power in cellular and FM bands (at 18 dBm) <sup>a</sup>	76–108 MHz	FM RX	—	TBD	—	dBm/Hz
	776–794 MHz		—	–169.8	—	dBm/Hz
	869–960 MHz	cdmaOne, GSM850	—	–170	—	dBm/Hz
	925–960 MHz	E-GSM	—	–170	—	dBm/Hz
	1570–1580 MHz	GPS	—	–170	—	dBm/Hz
	1805–1880 MHz	GSM1800	—	–170	—	dBm/Hz
	1930–1990 MHz	GSM1900, cdmaOne, WCDMA	—	–169	—	dBm/Hz
	2110–2170 MHz	WCDMA	—	–170	—	dBm/Hz
	2400–2483 MHz	BT/WLAN	—	–170	—	dBm/Hz
	2500–2570 MHz	Band 7	—	–168.5	—	dBm/Hz
	2300–2400 MHz	Band 40	—	–169	—	dBm/Hz
	2570–2620 MHz	Band 38	—	168.5	—	dBm/Hz
	2545–2575 MHz	XGP Band	—	–169	—	dBm/Hz
Harmonic level (at 17 dBm)	9.8–11.570 GHz	2 <sup>nd</sup> harmonic	—	–60	—	dBm/MHz
General spurs	1–8 GHz		—	–40	—	dBm/MHz
TX power at RF port for highest power level setting at 25°C with spectral mask and EVM compliance		<b>EVM Does Not Exceed</b>				
	OFDM, QPSK	–13 dB	2	5.2	—	dBm
	OFDM, 16-QAM	–19 dB	2	5.2	—	dBm
	OFDM, 64-QAM (R = 3/4)	–25 dB	2	5.2	—	dBm
	OFDM, 64-QAM (R = 5/6)	–27 dB	2	5.2	—	dBm
	OFDM, 256-QAM (R = 3/4, VHT)	–30 dB	2	4	—	dBm
	OFDM, 256-QAM (R = 5/6, VHT)	–32 dB	2	2	—	dBm
TX power control dynamic range	—		—	30	—	dB
Closed-loop TX power variation <sup>b</sup>	Over the full temperature and voltage ranges		—	—	±1.5	dB
Carrier suppression	—		15	—	—	dBc
Gain control step	—		—	0.25	—	dB
Return loss	Zo = 50Ω		—	TBD	—	dB

a. The cellular standards listed indicate only typical usages of that band in some countries. Other standards may also be used within those bands.

b. Applies to an 8 dBm to 20 dBm TX power output range with production PA trimming. Applies to a –10 dBm to 20 dBm TX power output range with PA trimming and open-loop power control (OLPC) calibration in production.

## 8.7 General Spurious Emissions Specifications

Table 32: General Spurious Emissions Specifications

Parameter	Condition/Notes		Min.	Typ.	Max.	Unit
Frequency range	—		2400	—	2500	MHz
General Spurious Emissions						
TX emissions	30 MHz < f < 1 GHz	RBW = 100 kHz	—	TBD	—	dBm
	1 GHz < f < 12.75 GHz	RBW = 1 MHz	—	TBD	—	dBm
	1.8 GHz < f < 1.9 GHz	RBW = 1 MHz	—	TBD	—	dBm
	5.15 GHz < f < 5.3 GHz	RBW = 1 MHz	—	TBD	—	dBm
RX/standby emissions	30 MHz < f < 1 GHz	RBW = 100 kHz	—	TBD	—	dBm
	1 GHz < f < 12.75 GHz	RBW = 1 MHz	—	TBD	—	dBm
	1.8 GHz < f < 1.9 GHz	RBW = 1 MHz	—	TBD	—	dBm
	5.15 GHz < f < 5.3 GHz	RBW = 1 MHz	—	TBD	—	dBm

## Chapter 9: System Power Consumption

**NOTE:** Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Unless otherwise stated, these values apply for the conditions specified in [Table 3, Recommended Operating Conditions and DC Characteristics](#).

### 9.1 WLAN Current Consumption

The WLAN current consumption measurements are shown in [Table 33](#).

All values in [Table 33](#) are with the Bluetooth core in reset (that is, Bluetooth is off).

**Table 33: Typical WLAN Power Consumption**

Mode	Bandwidth (MHz)	Band (GHz)	V <sub>bat</sub> = 3.6V mA	V <sub>io</sub> = 1.8V mA <sup>a</sup>
<b>Sleep Modes</b>				
OFF <sup>b</sup>	—	—	0.03	0.0
Sleep <sup>c</sup>	—	—	0.27	0.06
IEEE power save, DTIM 1 1 RX core <sup>d</sup>	20	2.4	1.55	0.08
IEEE power save, DTIM 3 1 RX core <sup>d</sup>	20	2.4	0.55	0.08
IEEE power save, DTIM 1 1 RX core <sup>d</sup>	20	5	1.7	0.08
IEEE power save, DTIM 3 1 RX core <sup>d</sup>	20	5	0.7	0.08
IEEE power save, DTIM 1 1 RX core <sup>d</sup>	40	5	1.7	0.08
IEEE power save, DTIM 3 1 RX core <sup>d</sup>	40	5	0.7	0.08
IEEE power save, DTIM 1 1 RX core <sup>d</sup>	80	5	1.8	0.08
IEEE power save, DTIM 3 1 RX core <sup>d</sup>	80	5	1.03	0.08
<b>Active Modes</b>				
<b>Transmit</b>				
CCK 1 chain <sup>e</sup>	20	2.4	450	3.2
1×1 MCS7, HT20	20	2.4	320	3.2
2×2 MCS15, HT20	20	2.4	550	3.2
1×1 MCS7, HT20	20	5	66	3.2
2×2 MCS15, HT20	20	5	100	3.2
1×1 MCS7, HT40	40	5	70	2.8
2×2 MCS15, HT40	40	5	105	2.8
MCS9, VHT80, NSS = 1	80	5	78	2.5
MCS9, VHT80, NSS = 2	80	5	120	2.5

**Table 33: Typical WLAN Power Consumption (Continued)**

Mode	Bandwidth (MHz)	Band (GHz)	V <sub>bat</sub> = 3.6V mA	V <sub>io</sub> = 1.8V mA <sup>a</sup>
<b>Receive</b>				
1×1 MCS7 HT20	20	2.4	28.3	1.45
2×2 MCS15 HT20	20	2.4	36.2	1.45
1×1 MCS7 HT20	20	5	49	1.6
2×2 MCS15 HT20	20	5	66	1.6
1×1 MCS7 HT40	40	5	55	1.7
2×2 MCS15 HT40	40	5	76	1.7
MCS9, VHT80, NSS = 1	80	5	65	1.9
MCS9, VHT80, NSS = 2	80	5	94	1.9

- a. Specified with all pins idle (not switching) and not driving any loads.
- b. WL\_REG\_ON, BT\_REG\_ON both low.
- c. Idle, not associated, or inter-beacon.
- d. Beacon Interval is 102.4 ms. Beacon duration is 1 ms at 1 Mbps (for 2.4 GHz) and 6 Mbps (for 5 GHz). Average current over 10 DTIM intervals.
- e. Output power per core at the chip RF port = TBD dBm.

## 9.2 Bluetooth Current Consumption

The Bluetooth and BLE current consumption measurements are shown in [Table 34](#).

**NOTE:** The WLAN core is in reset (WL\_REG\_ON = low) for all measurements provided in [Table 34](#).

**NOTE:** The BT current consumption numbers are measured based on GFSK TX output power = 13 dBm.

**Table 34: Bluetooth and BLE Current Consumption**

Operating Mode	VBAT (VBAT = 3.6V) Typical	VDDIO (VDDIO = 1.8V) Typical	Units
Sleep	38	168	μA
Standard 1.28s inquiry scan	205	180	μA
500 ms sniff master	190	180	μA
DM1/DH1	14	0.28	mA
DM3/DH3	17	0.28	mA
DM5/DH5	19	0.28	mA
3DH5/3DH1 master	17	0.28	mA
HV3 SCO	7	0.20	mA
BLE scan	152	180	μA
BLE adv. unconnectable 1s	130	180	μA
BLE connected 1s	107	180	μA

## Chapter 10: Package Information

### 10.1 WLCSP Coordinates

Table 35 lists the BCM4375 WLCSP coordinates by bump number. The table pertains to a bump-side view (that is, with the die facing up).

Table 35: BCM4375 WLCSP Coordinates by Bump Number

Bump	Net Name	Package Bump Side View (0, 0 center of die)	
		X-COORD	Y-COORD
1	VSS	2722.320	2952.405
2	VDD_AUX	−2477.520	2952.405
3	VSS	−2232.720	2952.405
4	VSS	−1987.920	2952.405
5	VSS	−1695.726	2952.405
6	RF_SW_CTRL_12	−1495.728	2952.405
7	RF_SW_CTRL_11	−1295.730	2952.405
8	RF_SW_CTRL_10	−1095.732	2952.405
9	VSS	−895.734	2952.405
10	VDD_TOP	286.254	2899.971
11	VSS	−2895.714	2779.011
12	VSS	−2599.920	2779.011
13	VSS	−2355.120	2779.011
14	VSS	−1924.020	2761.200
15	VDD_AUX	−1578.726	2752.407
16	RF_SW_CTRL_13	−1178.730	2752.407
17	VDDIO_RF	−978.732	2752.407
18	VSS	−778.734	2752.407
19	VDD_TOP	−95.742	2744.973
20	GPIO_16	104.256	2744.973
21	VDD_TOP	−295.740	2725.173
22	MODEHV	−495.738	2699.973
23	GPIO_19	304.254	2699.973
24	VSS	−1378.728	2662.407
25	VSS	−1756.620	2637.000
26	VSS	−1227.519	2499.975
27	VDDP_RF	−895.734	2499.975
28	VSS	−695.736	2499.975
29	VDDP_RF	−495.738	2499.975
30	VSS	−295.740	2499.975
31	VDD_AON	−95.742	2499.975

Table 35: BCM4375 WLCSP Coordinates by Bump Number (Continued)

Bump	Net Name	Package Bump Side View (0, 0 center of die)	
		X-COORD	Y-COORD
32	VSS	104.256	2499.975
33	VDD_AUX	304.254	2499.975
34	VSS	-1237.230	2299.977
35	VDD_AON	-1037.232	2299.977
36	VDD_AUX	-695.736	2299.977
37	VDDIO_RF	-495.738	2299.977
38	RF_SW_CTRL_18	-295.740	2299.977
39	VDD_AUX	-95.742	2299.977
40	GPIO_15	104.256	2299.977
41	GPIO_20	304.254	2299.977
42	VDD_RET_WL	1304.244	2299.977
43	RF_SW_CTRL_14	-1095.732	2099.979
44	RF_SW_CTRL_15	-895.734	2099.979
45	RF_SW_CTRL_16	-695.736	2099.979
46	RF_SW_CTRL_17	-495.738	2099.979
47	RF_SW_CTRL_19	-295.740	2099.979
48	GPIO_14	104.256	2099.979
49	GPIO_18	304.254	2099.979
50	PCI_PME_L	1304.244	2099.979
51	PCIE_CLKREQ_L	1504.242	2099.979
52	PERST_L	1704.240	2094.507
53	VDD_AUX	2104.236	2094.507
54	VDD18_UPI	2304.234	2094.507
55	VDD_TOP	-1237.230	1899.981
56	VSS	-1037.232	1899.981
57	VDDIO_RF	-495.738	1899.981
58	VSS	-295.740	1899.981
59	VDDIO	-95.742	1899.981
60	GPIO_13	104.256	1899.981
61	GPIO_17	304.254	1899.981
62	VSS	504.252	1899.981
63	VDD_AUX	704.250	1899.981
64	VDD_AUX	1104.246	1899.981
65	PACKAGEOPTION_0	1304.244	1899.981
66	PACKAGEOPTION_1	1504.242	1899.981
67	VDD_AON	1704.240	1894.509
68	PACKAGEOPTION_2	1904.238	1894.509
69	VDD_AUX	2104.236	1894.509
70	VDDIO	2394.234	1899.981
71	VSS	2594.232	1894.581

**Table 35: BCM4375 WLCSP Coordinates by Bump Number (Continued)**

Bump	Net Name	Package Bump Side View (0, 0 center of die)	
		X-COORD	Y-COORD
72	FLL_VDDIO	2826.990	1762.983
73	VSS	-1237.230	1699.983
74	VSS	-1037.232	1699.983
75	VSS	-837.234	1699.983
76	VSS	-637.236	1699.983
77	VSS	-437.238	1699.983
78	VSS	-95.742	1699.983
79	VSS	104.256	1699.983
80	VDDIO	304.254	1699.983
81	VSS	704.250	1699.983
82	VDD_TOP	904.248	1699.983
83	JTAG_SEL	1104.246	1699.983
84	VSS	1304.244	1699.983
85	VDDIO	1504.242	1699.983
86	GPIO_8	1904.238	1694.511
87	GPIO_7	2104.236	1694.511
88	GPIO_6	2394.234	1699.983
89	VSS	2626.992	1558.485
90	VDD_TOP	2826.990	1558.485
91	VSS	-1062.972	1499.985
92	VSS	-862.974	1499.985
93	VSS	-662.976	1499.985
94	VSS	-462.978	1499.985
95	VSS	-262.980	1499.985
96	VSS	-62.982	1499.985
97	VDD_MAIN	137.016	1499.985
98	VSS	337.014	1499.985
99	VSS	737.010	1499.985
100	VSS	937.008	1499.985
101	VSS	1137.006	1499.985
102	VDD_DIG	1337.004	1499.985
103	GPIO_11	1537.002	1499.985
104	VDD_AON	1936.998	1494.513
105	GPIO_10	2136.996	1494.513
106	GPIO_9	2381.994	1499.985
107	GPIO_1	2626.992	1358.487
108	GPIO_0	2826.990	1358.487
109	VSS	-1240.470	1299.987
110	VSS	-1040.472	1299.987
111	VDD_RET_WL	-840.474	1299.987

**Table 35: BCM4375 WLCSP Coordinates by Bump Number (Continued)**

Bump	Net Name	Package Bump Side View (0, 0 center of die)	
		X-COORD	Y-COORD
112	VDD_MAIN	–462.978	1299.987
113	VSS	337.014	1299.987
114	LHL_GPIO1	537.012	1299.987
115	VDD_AON	937.008	1299.987
116	VDD_RET_WL	1137.006	1299.987
117	GPIO_12	1337.004	1299.987
118	VDDIO	1537.002	1299.987
119	VSS	1737.000	1299.987
120	VDD_AON	2136.996	1294.515
121	GPIO_2	2381.994	1299.987
122	VSS	2559.492	1158.489
123	VDD_TOP	2759.490	1158.489
124	VSS	–1240.470	1099.989
125	VDD_MAIN	–1040.472	1099.989
126	VSS	–840.474	1099.989
127	VSS	–462.978	1099.989
128	VSS	–262.980	1099.989
129	VSS	–62.982	1099.989
130	VSS	137.016	1099.989
131	VSS	337.014	1099.989
132	LHL_GPIO0	537.012	1099.989
133	LHL_GPIO2	737.010	1099.989
134	VSS	937.008	1099.989
135	VSS	1137.006	1099.989
136	OTP_VDD1P8	1337.004	1099.989
137	VDD_DIG	1537.002	1099.989
138	VSS	1737.000	1099.989
139	GPIO_4	1936.998	1099.989
140	GPIO_3	2136.996	1094.517
141	VSS	2336.994	1099.989
142	VDD_AON	–1240.470	899.991
143	VSS	–840.474	899.991
144	VSS	–462.978	899.991
145	VSS	–262.980	899.991
146	VSS	–62.982	899.991
147	VSSC	337.014	899.991
148	LHL_VDDO	537.012	899.991
149	LHL_GPIO3	737.010	899.991
150	VSS	1137.006	899.991
151	VSS	1337.004	899.991

Table 35: BCM4375 WLCSP Coordinates by Bump Number (Continued)

Bump	Net Name	Package Bump Side View (0, 0 center of die)	
		X-COORD	Y-COORD
152	VDD_TOP	1936.998	899.991
153	GPIO_5	2136.996	894.519
154	VSS	-1240.470	699.993
155	VSS	-1040.472	699.993
156	VSS	-840.474	699.993
157	VSS	-462.978	699.993
158	VSS	-262.980	699.993
159	VSS	-62.982	699.993
160	VSS	137.016	699.993
161	LPO_IN	337.014	699.993
162	VSSC	537.012	699.993
163	VSSC	937.008	699.993
164	VDD_TOP	1137.006	699.993
165	VSS	1337.004	699.993
166	VDD_DIG	1537.002	699.993
167	VSS	1737.000	699.993
168	VSS	1936.998	699.993
169	VDD_AON	2236.995	699.993
170	VDD_TOP	-1240.470	499.995
171	VSS	-1040.472	499.995
172	VSS	-840.474	499.995
173	VDD_AON	-462.978	499.995
174	VDD_TOP	-262.980	499.995
175	VSS	137.016	499.995
176	VSSC	337.014	499.995
177	VSSC	937.008	499.995
178	VSS	1337.004	499.995
179	VSS	1737.000	499.995
180	VSS	1936.998	499.995
181	VSS	2136.996	499.995
182	VSS	-1240.470	299.997
183	VSS	-862.974	299.997
184	VDD_MAIN	-662.976	299.997
185	VSS	-462.978	299.997
186	VSS	-262.980	299.997
187	VDD_MAIN	137.016	299.997
188	VSSC	337.014	299.997
189	LHL_XTALO	537.012	299.997
190	LHL_XTALI	737.010	299.997
191	VDD_AON	937.008	299.997

Table 35: BCM4375 WLCSP Coordinates by Bump Number (Continued)

Bump	Net Name	Package Bump Side View (0, 0 center of die)	
		X-COORD	Y-COORD
192	VSS	1337.004	299.997
193	VDD_DIG	1537.002	299.997
194	VDD_TOP	1936.998	299.997
195	VSS	2236.995	299.997
196	VSS	-1240.470	99.999
197	VSS	-1040.472	99.999
198	VSS	-840.474	99.999
199	VSS	-462.978	99.999
200	VSS	-262.980	99.999
201	VSS	137.016	99.999
202	PAD_AVDD1P0	337.014	99.999
203	VSSC	537.012	99.999
204	VSSC	737.010	99.999
205	VSS	937.008	99.999
206	VSS	1137.006	99.999
207	VSS	1337.004	99.999
208	VSS	1537.002	99.999
209	VSS	1737.000	99.999
210	VSS	1936.998	99.999
211	VSS	2136.996	99.999
212	VSS	-1040.472	-99.999
213	VSS	-840.474	-99.999
214	VSS	-462.978	-99.999
215	VSS	-262.980	-99.999
216	VSS	-62.982	-99.999
217	VSS	137.016	-99.999
218	PAD_AVSS	337.014	-99.999
219	VSS	537.012	-99.999
220	VSS	737.010	-99.999
221	VSS	937.008	-99.999
222	VSS	1137.006	-99.999
223	VSS	1337.004	-99.999
224	VDD_DIG	1737.000	-99.999
225	VSS	2136.996	-99.999
226	VSS	2426.994	-99.999
227	RF_SW_CTRL_0	2649.492	-99.999
228	VDDIO_RF	2871.990	-99.999
229	VSS	-1162.971	-299.997
230	VSS	-962.973	-299.997
231	VDD_MAIN	-762.975	-299.997

Table 35: BCM4375 WLCSP Coordinates by Bump Number (Continued)

Bump	Net Name	Package Bump Side View (0, 0 center of die)	
		X-COORD	Y-COORD
232	VDD_MAIN	-462.978	-299.997
233	VSS	-262.980	-299.997
234	VSS	-62.982	-299.997
235	VDD_MAIN	316.377	-299.997
236	VDD_TOP	937.008	-299.997
237	VDD_AON	1337.004	-299.997
238	VSS	1737.000	-299.997
239	VSS	1936.998	-299.997
240	RF_SW_CTRL_1	2136.996	-299.997
241	VSS	2871.990	-299.997
242	VDD_AON	-1083.609	-499.995
243	VSS	-883.611	-499.995
244	VSS	-683.613	-499.995
245	VSS	-283.617	-499.995
246	VSS	-83.619	-499.995
247	VSS	316.377	-499.995
248	VDD_AON	516.375	-499.995
249	VSS	916.371	-499.995
250	VSS	1116.369	-499.995
251	VSS	1316.367	-499.995
252	VSS	1716.363	-499.995
253	VDD_RET_WL	1916.361	-499.995
254	RF_SW_CTRL_4	2116.359	-499.995
255	RF_SW_CTRL_2	2427.894	-499.995
256	VDD_AON	2649.492	-499.995
257	VDD_DIG	2872.890	-499.995
258	VDD_TOP	-1083.609	-699.993
259	VSS	-883.611	-699.993
260	VSS	-683.613	-699.993
261	VSS	-283.617	-699.993
262	VSS	-83.619	-699.993
263	VSS	316.377	-699.993
264	VSS	516.375	-699.993
265	VDD_MAIN	716.373	-699.993
266	VSS	916.371	-699.993
267	VSS	1316.367	-699.993
268	VDD_TOP	1516.365	-699.993
269	VSS	1716.363	-699.993
270	VSS	1916.361	-699.993
271	VSS	2116.359	-699.993

Table 35: BCM4375 WLCSP Coordinates by Bump Number (Continued)

Bump	Net Name	Package Bump Side View (0, 0 center of die)	
		X-COORD	Y-COORD
272	RF_SW_CTRL_7	2316.357	-699.993
273	RF_SW_CTRL_3	2516.355	-699.993
274	VDD_TOP	2716.353	-699.993
275	VSS	-1083.609	-899.991
276	VSS	-883.611	-899.991
277	VSS	-683.613	-899.991
278	VSS	-283.617	-899.991
279	VSS	-83.619	-899.991
280	VSS	116.379	-899.991
281	VSS	316.377	-899.991
282	VSS	516.375	-899.991
283	VSS	916.371	-899.991
284	VSS	1316.367	-899.991
285	VSS	1716.363	-899.991
286	RF_SW_CTRL_9	2116.359	-899.991
287	RF_SW_CTRL_6	2316.357	-899.991
288	VDDP_RF	2516.355	-899.991
289	VSS	2716.353	-899.991
290	VSS	-1083.609	-1099.989
291	VSS	-683.613	-1099.989
292	VSS	-283.617	-1099.989
293	VDD_MAIN	716.373	-1099.989
294	VSS	916.371	-1099.989
295	VSS	1116.369	-1099.989
296	VSS	1316.367	-1099.989
297	VSS	1516.365	-1099.989
298	VDD_DIG	1716.363	-1099.989
299	VSS	1916.361	-1099.989
300	VDD_RET_WL	2116.359	-1099.989
301	RF_SW_CTRL_8	2316.357	-1099.989
302	RF_SW_CTRL_5	2643.354	-1099.989
303	VDD_AON	-1083.609	-1299.987
304	VSS	-683.613	-1299.987
305	VDD_MAIN	-283.617	-1299.987
306	VSS	-83.619	-1299.987
307	VSS	116.379	-1299.987
308	VSS	316.377	-1299.987
309	VSS	516.375	-1299.987
310	VSS	716.373	-1299.987
311	VSS	916.371	-1299.987

Table 35: BCM4375 WLCSP Coordinates by Bump Number (Continued)

Bump	Net Name	Package Bump Side View (0, 0 center of die)	
		X-COORD	Y-COORD
312	VSS	1516.365	-1299.987
313	VSS	1716.363	-1299.987
314	VDDIO_RF	2116.359	-1299.987
315	RF_SW_CTRL_20	2316.357	-1299.987
316	VDDP_RF	2516.355	-1299.987
317	MODEHV1	2716.353	-1299.987
318	VSS	-1083.609	-1499.985
319	VSS	-883.611	-1499.985
320	VSS	-683.613	-1499.985
321	VSS	-283.617	-1499.985
322	VSS	-83.619	-1499.985
323	VSS	116.379	-1499.985
324	VSS	716.373	-1499.985
325	VSS	916.371	-1499.985
326	VSS	1116.369	-1499.985
327	VDD_AON	1316.367	-1499.985
328	VSS	1516.365	-1499.985
329	VDD_RET_WL	1716.363	-1499.985
330	VSS	1916.361	-1499.985
331	VDD_DIG	2316.357	-1499.985
332	VSS	2516.355	-1499.985
333	VDD_AON	2716.353	-1499.985
334	VSS	-1083.609	-1699.983
335	VSS	-683.613	-1699.983
336	VDD_MAIN	-483.615	-1699.983
337	VSS	-283.617	-1699.983
338	VSS	-83.619	-1699.983
339	BT_VDDC	116.379	-1699.983
340	BT_VSSC	316.377	-1699.983
341	BT_VSSC	516.375	-1699.983
342	BT_VSSC	716.373	-1699.983
343	BT_VSSC	1316.367	-1699.983
344	VSS	1516.365	-1699.983
345	VSS	1806.363	-1699.983
346	VDD_TOP	2006.361	-1699.983
347	RF_SW_CTRL_21	2206.359	-1699.983
348	RF_SW_CTRL_22	2406.357	-1699.983
349	RF_SW_CTRL_24	2606.355	-1699.983
350	RF_SW_CTRL_23	2806.353	-1699.983
351	VDD_TOP	-1083.609	-1899.981

Table 35: BCM4375 WLCSP Coordinates by Bump Number (Continued)

Bump	Net Name	Package Bump Side View (0, 0 center of die)	
		X-COORD	Y-COORD
352	BT_VSSC	-883.611	-1899.981
353	VSS	-683.613	-1899.981
354	VSS	-483.615	-1899.981
355	VSS	-238.617	-1899.981
356	BT_VDDCLDO	268.875	-1899.981
357	BT_VSSC	493.875	-1899.981
358	BT_VSSC	716.373	-1899.981
359	BT_VSSC	916.371	-1899.981
360	BT_VSSC	1116.369	-1899.981
361	BT_VSSC	1316.367	-1899.981
362	BT_GPIO_3	1516.365	-1899.981
363	BT_VSSC	1806.363	-1899.981
364	BT_VDDC_AAON	2006.361	-1899.981
365	BT_VDDCLDO	2206.359	-1899.981
366	BT_SLIMBUS_DT	2406.357	-1899.981
367	BT_VDDCG	2606.355	-1899.981
368	BT_SLIMBUS_CK	2806.353	-1899.981
369	VSS	-1062.630	-2099.979
370	BT_VDDCLDO	916.371	-2099.979
371	BT_VSSC	1116.369	-2099.979
372	BT_VDDCLDO	1316.367	-2099.979
373	BT_AJTAG_TCK	1516.365	-2099.979
374	BT_VDDCLDO	1716.363	-2099.979
375	BT_I2S_CLK	2006.361	-2099.979
376	BT_UART_CTS_N	2206.359	-2099.979
377	BT_HOST_WAKE	2406.357	-2099.979
378	BT_VSSC	2606.355	-2099.979
379	BT_VDDO	2806.353	-2099.979
380	VDD_TOP	-1062.630	-2299.977
381	BT_VDDC	916.371	-2299.977
382	BT_VSSC	1116.369	-2299.977
383	BT_I2S_DO	1316.367	-2299.977
384	BT_PCM_SYNC	1516.365	-2299.977
385	BT_VSSC	1806.363	-2299.977
386	BT_VDDMEMPLDO	2006.361	-2299.977
387	BT_PCM_CLK	2206.359	-2299.977
388	BT_UART_RTS_N	2406.357	-2299.977
389	BT_UART_TXD	2606.355	-2299.977
390	BT_VDDC	2806.353	-2299.977
391	VDD_AON	-1062.630	-2499.975

**Table 35: BCM4375 WLCSP Coordinates by Bump Number (Continued)**

Bump	Net Name	Package Bump Side View (0, 0 center of die)	
		X-COORD	Y-COORD
392	BT_VSSC	916.371	-2499.975
393	BT_VSSC	1116.369	-2499.975
394	BT_VSSC	1316.367	-2499.975
395	BT_VSSC	1516.365	-2499.975
396	BT_VDDC	1806.363	-2499.975
397	BT_PCM_OUT	2006.361	-2499.975
398	BT_PCM_IN	2206.359	-2499.975
399	BT_UART_RXD	2406.357	-2499.975
400	BT_I2S_WS	2606.355	-2499.975
401	BT_I2S_DI	2806.353	-2499.975
402	VSS	-1062.630	-2699.973
403	BT_AJTAG_TDO	1806.363	-2739.501
404	BT_AJTAG_TDI	2006.361	-2739.501
405	BT_AJTAG_TMS	2206.359	-2739.501
406	BT_TM1	2406.357	-2739.501
407	BT_VSSC	2606.355	-2739.501
408	BT_DEV_WAKE	2824.353	-2739.501
409	VSS	-1062.630	-2899.971
410	BT_GPIO_2	1681.488	-2939.499
411	BT_CLK_REQ	1881.486	-2939.499
412	BT_GPIO_4	2081.484	-2939.499
413	BT_GPIO_5	2281.482	-2939.499
414	BT_VSSC	2481.480	-2939.499
415	BT_VDDO	2685.978	-2939.499
416	BT_VDDB	-31.617	-1899.981
417	PAD_I_TVDD1P0	2692.706	318.393
418	PAD_I_PVDD1P0	2692.706	718.389
419	PAD_O_TDP0	2892.704	318.393
420	PAD_O_TESTP	2492.708	118.395
421	PAD_I_RGND	2892.704	918.392
422	PAD_I_RVDD1P0	2692.706	918.392
423	PAD_I_REFCLKN	2492.708	518.391
424	PAD_I_RDP0	2892.704	718.389
425	PAD_I_RDN0	2892.704	518.391
426	PAD_I_REFCLKP	2492.708	718.389
427	PAD_I_TGND	2692.706	118.395
428	PAD_O_TDN0	2892.704	118.395
429	PAD_I_PGND	2492.708	918.392
430	PAD_O_TESTN	2492.708	318.393
431	VDDOUT_RFLDO_SNS	504.252	2948.499

Table 35: BCM4375 WLCSP Coordinates by Bump Number (Continued)

Bump	Net Name	Package Bump Side View (0, 0 center of die)	
		X-COORD	Y-COORD
432	ASR_VDDBAT5	2104.236	2948.499
433	CSR_VDDBAT5	2304.234	2694.501
434	CSR_VDDBAT5	2304.234	2494.503
435	PVSSC	2704.230	2694.501
436	LDO_VDD0P9	2904.228	2694.501
437	PVSSA	1704.240	2948.499
438	CSR_VLX	2504.232	2694.501
439	PVSSA	1704.240	2694.501
440	ASR_VLX	1904.238	2948.499
441	PVSSC	2704.230	2494.503
442	VDDOUT_MISCLDO	1304.244	2548.503
443	CSR_VLX	2504.232	2948.499
444	VSSC	1504.242	2348.505
445	VDDOUT_SWCORE	2904.228	2494.503
446	CSR_VLX	2504.232	2294.505
447	PVSSC	2704.230	2094.507
448	BT_REG_ON	904.248	2148.507
449	VDDOUT_BTLDO_SNS	1104.246	2948.499
450	PMU_AVSS	1504.242	2548.503
451	VDDOUT_BT3P3	1104.246	2548.503
452	VDDOUT_BT3P3	1104.246	2748.501
453	VDDOUT_RF3P3	504.252	2148.507
454	WL_REG_ON	704.250	2148.507
455	PMU_VDDIOP	1504.242	2748.501
456	LDO_VDDBAT5	704.250	2348.505
457	VDDOUT_RF3P3	504.252	2348.505
458	VDDOUT_RF3P3	504.252	2748.501
459	VDDOUT_RF3P3	504.252	2548.503
460	CSR_VLX	2504.232	2494.503
461	PVSSC	2704.230	2294.505
462	CSR_VLX	2504.232	2094.507
463	PMU_VDDIOA	1304.244	2748.501
464	VDDOUT_MEMLPLDO	1304.244	2948.499
465	VDDOUT_AON	2904.228	2294.505
466	PVSSA	1704.240	2494.503
467	VDDOUT_BT3P3	1104.246	2348.505
468	LDO_VDDBAT5	704.250	2748.501
469	LDO_VDDBAT5	704.250	2948.499
470	LDO_VDDBAT5	704.250	2548.503
471	LDO_VDDBAT5	904.248	2348.505

Table 35: BCM4375 WLCSP Coordinates by Bump Number (Continued)

Bump	Net Name	Package Bump Side View (0, 0 center of die)	
		X-COORD	Y-COORD
472	LDO_VDDBAT5	904.248	2548.503
473	LDO_VDDBAT5	904.248	2748.501
474	LDO_VDDBAT5	904.248	2948.499
475	NC	1104.246	2148.507
476	CSR_VDDBAT5	2304.234	2948.499
477	ASR_VDDBAT5	2104.236	2494.503
478	ASR_VDDBAT5	2104.236	2694.501
479	ASR_VLX	1904.238	2494.503
480	ASR_VLX	1904.238	2294.505
481	ASR_VLX	1904.238	2094.507
482	LDO_VDD1P12	1504.242	2948.499
483	ASR_VLX	1904.238	2694.501
484	PVSSC	2704.230	2948.499
485	PVSSA	1704.240	2294.505
486	VSSC	2104.236	2294.505
487	PMU_AVSS	2304.234	2294.505
488	VDD_V1P8_CORE1_MAIN	-1693.823	-605.633
489	VDD_V1P8_CORE0_MAIN	-2211.561	-2952.504
490	PMU_TX_VDD_V1P12_CORE0_MAIN	-2473.628	-2952.504
491	PMU_TX_VDD_V1P12_CORE1_MAIN	-1985.117	-605.633
492	AFE_VDD_V1P12_CORE0_MAIN	-2342.664	-2801.214
493	AFE_VDD_V1P12_CORE1_MAIN	-1537.826	-731.817
494	RADIO_GND	-2247.611	-368.667
495	RADIO_GND	-1553.391	2264.508
496	RADIO_GND	-1706.207	1682.136
497	RADIO_GND	-2432.840	593.609
498	RADIO_GND	-2847.618	-145.652
499	RADIO_GND	-2150.528	337.518
500	RADIO_GND	-2150.519	66.911
501	RADIO_GND	-2150.528	660.146
502	RADIO_GND	-2350.526	924.138
503	RADIO_GND	-2905.029	465.827
504	RADIO_GND	-1553.391	80.771
505	RADIO_GND	-1512.936	-2738.403
506	RADIO_GND	-2150.528	885.951
507	RADIO_GND	-2293.128	1399.113
508	RADIO_GND	-1737.738	-350.492
509	RADIO_GND	-2905.029	2215.832
510	VCO_VDD_V1P12_MAIN	-1618.295	-1538.897
511	PMU_VDD_V3P3_CORE1_MAIN	-1381.829	-605.633

Table 35: BCM4375 WLCSP Coordinates by Bump Number (Continued)

Bump	Net Name	Package Bump Side View (0, 0 center of die)	
		X-COORD	Y-COORD
512	SYNTH_VDD_V1P12_MAIN	-1822.136	-1516.248
513	PMU_VDD_V3P3_CORE0_MAIN	-2623.293	-2819.691
514	RADIO_GND	-1312.938	-2738.403
515	RADIO_GND	-1512.936	-1107.189
516	RADIO_GND	-1312.938	-1107.189
517	RADIO_GND	-1363.131	-2196.855
518	RADIO_GND	-1356.485	-1710.230
519	RADIO_GND	-2505.033	-1821.654
520	RADIO_GND	-2026.665	-1407.969
521	RADIO_GND	-2905.029	-1821.654
522	RADIO_GND	-2705.031	-1821.654
523	RADIO_GND	-2246.544	-782.933
524	RADIO_GND	-2752.488	-845.217
525	RADIO_GND	-1857.515	-760.212
526	RADIO_GND	-2668.293	-2364.669
527	RADIO_GND	-2461.811	-2353.262
528	RADIO_GND	-2584.877	-2045.741
529	RADIO_GND	-2584.877	-985.946
530	RADIO_GND	-2668.293	-1304.874
531	RADIO_GND	-1937.736	-350.492
532	RADIO_GND	-2847.618	1604.354
533	PAOUT_5G_CORE0_MAIN	-2905.029	-2366.046
534	RFIN_5G_CORE0_MAIN	-2905.029	-2166.048
535	GPAIO_CORE0_MAIN	-1865.556	-2608.947
536	RADIO_GND	-2150.528	2617.506
537	RADIO_GND	-2447.609	-368.667
538	RADIO_GND	-2604.951	695.543
539	RADIO_GND	-1886.625	-18.257
540	RADIO_GND	-2808.770	117.333
541	TSSI5G_CORE0_MAIN	-1665.558	-2608.947
542	GPAIO_CORE1_MAIN	-1865.556	-1236.645
543	TSSI5G_CORE1_MAIN	-1665.558	-1236.645
544	RADIO_GND	-2905.029	-2793.488
545	PAOUT_5G_CORE1_MAIN	-2905.029	-1306.251
546	PA_VDD_V3P3_CORE1_MAIN	-2731.923	-1591.686
547	RADIO_GND	-2153.196	-2688.953
548	SYNTH_VDD_V3P3_MAIN	-1713.231	-2350.814
549	RADIO_GND	-2509.425	-2651.481
550	RADIO_GND	-2150.528	2087.505
551	RADIO_GND	-1537.740	-350.492

Table 35: BCM4375 WLCSP Coordinates by Bump Number (Continued)

Bump	Net Name	Package Bump Side View (0, 0 center of die)	
		X-COORD	Y-COORD
552	PA_VDD_V3P3_CORE0_MAIN	-2731.923	-2651.481
553	RADIO_GND	-2023.304	-2424.294
554	RADIO_GND	-2209.491	-1921.653
555	VCO_VDD_V3P3_MAIN	-1776.623	-2160.590
556	RADIO_GND	-1761.764	-1710.230
557	RADIO_GND	-2461.811	-1293.467
558	RADIO_GND	-2509.425	-1591.686
559	RADIO_GND	-2253.731	-1719.486
560	PA2G_VDD_V3P3_C0_AUX	-2358.950	39.321
561	RADIO_GND	-1553.391	280.769
562	RADIO_GND	-2604.951	2445.548
563	RADIO_GND	-2808.770	1867.338
564	RFIN_5G_CORE1_MAIN	-2905.029	-1106.253
565	RADIO_GND	-2150.528	2297.858
566	RADIO_GND	-2432.840	2343.614
567	RADIO_GND	-1553.391	2064.510
568	RADIO_GND	-1805.027	713.376
569	RADIO_GND	-1886.625	2363.504
570	RADIO_GND	-1455.026	990.500
571	RADIO_GND	-2905.029	1000.440
572	RADIO_GND	-2842.938	1190.858
573	AFE_VDD_V1P12_AUX	-2642.931	1188.761
574	RADIO_GND	-2705.022	998.640
575	RADIO_GND	-2264.324	-2424.407
576	PA2G_VDD_V3P3_C1_AUX	-2358.950	1789.326
577	RADIO_GND	-2264.324	-1364.612
578	RADIO_GND	-1759.622	952.182
579	RADIO_GND	-2093.139	1415.471
580	RADIO_GND	-1906.205	1682.136
581	TX_VDD_V1P12_C0_AUX	-2388.623	334.062
582	RADIO_GND	-1553.391	1864.512
583	RADIO_GND	-1553.391	480.767
584	TX_VDD_V1P12_C1_AUX	-2388.623	2084.067
585	PAOUT_5G_C1_AUX	-2795.342	2383.187
586	GENERAL_VDD_V3P3_AUX	-2493.126	1322.159
587	PA2G_VDD_V3P3_C0_AUX	-2679.939	-36.045
588	PA2G_VDD_V3P3_C1_AUX	-2679.939	1713.960
589	PMU_VDD_V1P12_AUX	-2150.528	1112.850
590	RFIN_2G_C0_AUX	-2847.618	-359.150
591	RFIN_2G_C1_AUX	-2847.618	1390.856

Table 35: BCM4375 WLCSP Coordinates by Bump Number (Continued)

Bump	Net Name	Package Bump Side View (0, 0 center of die)	
		X-COORD	Y-COORD
592	AFE_VDD_V1P8_C0_AUX	-1455.026	-119.228
593	AFE_VDD_V1P8_C1_AUX	-1455.026	2464.506
594	EXT_TSSIA_C0_AUX	-1886.625	426.740
595	EXT_TSSIA_C1_AUX	-1886.625	1918.508
596	EXT_TSSIG_GPAIO_C0_AUX	-1886.625	226.742
597	EXT_TSSIG_GPAIO_C1_AUX	-1886.625	2118.506
598	RFIN_5G_C1_AUX	-2905.029	2550.447
599	PAOUT_2G_C0_AUX	-2771.033	317.327
600	PAOUT_2G_C1_AUX	-2771.033	2067.332
601	PAOUT_5G_C0_AUX	-2795.342	633.182
602	RFIN_5G_C0_AUX	-2905.029	800.442
603	TX_VDD_V3P3_C0_AUX	-2247.611	-133.088
604	TX_VDD_V3P3_C1_AUX	-2247.611	1616.918
605	VCO_VDD_V1P12_AUX	-1425.024	1548.248
606	SYNTH_VDD_V1P12_AUX	-1455.026	790.502
607	TX_VDD_V1P12_C0_AUX	-2583.108	389.097
608	TX_VDD_V1P12_C1_AUX	-2583.108	2139.102
609	RADIO_GND	-1404.639	-2505.780
610	RADIO_GND	-1735.493	-2901.645
611	RADIO_GND	-2253.731	-2121.651
612	RADIO_GND	-1559.124	-2047.388
613	RADIO_GND	-1735.493	-943.547
614	RADIO_GND	-2646.414	-645.219
615	RADIO_GND	-2184.570	-582.935
616	RADIO_GND	-2384.568	-976.676
617	RADIO_GND	-2218.280	-1088.829
618	RADIO_GND	-1312.938	-907.191
619	RADIO_GND	-1284.111	-1510.232
620	RADIO_GND	-1312.938	-2938.401
621	RADIO_GND	-2846.412	-645.219
622	RADIO_GND	-2774.129	-2952.504
623	I_PAD_BT_RFVSS	-789.444	-2769.125
624	I_PAD_BT_RFVSS	-739.782	-2407.352
625	I_PAD_BT_LDOVDD_V1P12	-729.482	-2202.503
626	O_PAD_BT_RFOP	-690.017	-2952.504
627	I_PAD_BT_RFVSS	-512.681	-2492.901
628	O_PAD_BT_13DBMOP	-486.990	-2724.399
629	O_PAD_BT_RFTEST	-325.859	-2086.704
630	O_PAD_BT_20DBMOP	-151.110	-2772.063
631	I_PAD_BT_IFVSS	-121.401	-2086.704

**Table 35: BCM4375 WLCSP Coordinates by Bump Number (Continued)**

Bump	Net Name	Package Bump Side View (0, 0 center of die)	
		X-COORD	Y-COORD
632	I_PAD_BT_VCOVSS	-84.357	-2324.187
633	I_PAD_BT_PAVSS	-80.132	-2580.935
634	I_PAD_BT_PAVSS	-40.271	-2952.504
635	I_PAD_BT_PAVSS	68.553	-2784.699
636	I_PAD_BT_VCOVSS	118.742	-2427.804
637	I_PAD_BT_IFVSS	158.076	-2086.704
638	I_PAD_BT_PAVDD_V3P3	203.535	-2952.504
639	I_PAD_BT_PAVSS	303.795	-2650.896
640	I_PAD_BT_IFVSS	358.074	-2086.704
641	I_PAD_BT_PAVDD_V3P3	403.533	-2952.504
642	I_PAD_BT_PAVSS	582.696	-2845.350
643	I_PAD_BT_PLLVSS	584.672	-2086.704
644	I_PAD_BT_PLLVSS	608.738	-2404.179
645	I_PAD_XTAL_GND	844.979	-2947.104
646	O_PAD_XTAL_XON	1044.977	-2952.504
647	I_PAD_XTAL_GND	1044.977	-2752.506
648	I_PAD_XTAL_XOP	1244.975	-2952.504
649	I_PAD_XTAL_GND	1244.975	-2752.506
650	I_PAD_VDD_XTAL	1444.973	-2952.504
651	I_PAD_XTAL_VDD_V1P12	1444.973	-2752.506

## 10.2 Signal Descriptions

Table 36 provides the signal name, type, and description of each pin in the BCM4375. The symbols shown under Type indicate pin directions (I/O = bidirectional, I = input, O = output) and the internal pull-up/pull-down characteristics (PU = weak internal pull-up resistor and PD = weak internal pull-down resistor), if any.

**Table 36: BCM4375 WLCSP Signal Descriptions**

Signal Name	Bump	Type	Description
<b>WLAN and Bluetooth Receive RF Signal Interface</b>			
EXT_TSSIA_C0_AUX	594	O	5 GHz TSSI CORE0 auxiliary
EXT_TSSIA_C1_AUX	595	O	5 GHz TSSI CORE1 auxiliary
EXT_TSSIG_GPAIO_C0_AUX	596	O	GPIO or 2.4 GHz TSSI CORE0 auxiliary
EXT_TSSIG_GPAIO_C1_AUX	597	O	GPIO or 2.4 GHz TSSI CORE1 auxiliary
GPAIO_CORE0_MAIN	535	I/O	Core 0 analog GPIO (main slice)
GPAIO_CORE1_MAIN	542	I/O	Core 1 analog GPIO (main slice)
PAOUT_2G_C0_AUX	599	O	2.4 GHz WLAN auxiliary CORE0 PA output
PAOUT_2G_C1_AUX	600	O	2.4 GHz WLAN auxiliary CORE1 PA output
PAOUT_5G_C0_AUX	601	O	5 GHz WLAN auxiliary CORE0 PA output
PAOUT_5G_C1_AUX	585	O	5 GHz WLAN auxiliary CORE1 PA output.
PAOUT_5G_CORE0_MAIN	533	O	5 GHz WLAN main CORE0 PA output
PAOUT_5G_CORE1_MAIN	545	O	5 GHz WLAN main CORE1 PA output
RFIN_2G_C0_AUX	590	I	2.4 GHz Bluetooth and WLAN auxiliary CORE0 receiver shared input.
RFIN_2G_C1_AUX	591	I	2.4 GHz Bluetooth and WLAN auxiliary CORE1 receiver shared input.
RFIN_5G_C0_AUX	602	I	5 GHz WLAN auxiliary CORE0 receiver input
RFIN_5G_C1_AUX	598	I	5 GHz WLAN auxiliary CORE1 receiver input
RFIN_5G_CORE0_MAIN	534	I	5 GHz WLAN main CORE0 receiver input
RFIN_5G_CORE1_MAIN	564	I	5 GHz WLAN main CORE1 receiver input
TSSI5G_CORE0_MAIN	541	O	5 GHz TSSI CORE0 main
TSSI5G_CORE1_MAIN	543	O	5 GHz TSSI CORE1 main

Table 36: BCM4375 WLCSP Signal Descriptions (Continued)

Signal Name	Bump	Type	Description
<b>RF Switch Control Lines</b>			
RF_SW_CTRL_0	227	O	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
RF_SW_CTRL_1	240	O	
RF_SW_CTRL_2	255	O	
RF_SW_CTRL_3	273	O	
RF_SW_CTRL_4	254	O	
RF_SW_CTRL_5	302	O	
RF_SW_CTRL_6	287	O	
RF_SW_CTRL_7	272	O	
RF_SW_CTRL_8	301	O	
RF_SW_CTRL_9	286	O	
RF_SW_CTRL_10	8	O	
RF_SW_CTRL_11	7	O	
RF_SW_CTRL_12	6	O	
RF_SW_CTRL_13	16	O	
RF_SW_CTRL_14	43	O	
RF_SW_CTRL_15	44	O	
RF_SW_CTRL_16	45	O	
RF_SW_CTRL_17	46	O	
RF_SW_CTRL_18	38	O	
RF_SW_CTRL_19	47	O	
RF_SW_CTRL_20	315	O	
RF_SW_CTRL_21	347	O	
RF_SW_CTRL_22	348	O	
RF_SW_CTRL_23	350	O	
RF_SW_CTRL_24	349	O	

Table 36: BCM4375 WLCSP Signal Descriptions (Continued)

Signal Name	Bump	Type	Description
<b>WLAN PCI Express Interface</b>			
PAD_I_RDN0	425	I	Receiver differential pair (×1 lane).
PAD_I_RDP0	424	I	
PAD_I_REFCLKN	423	I	PCIe differential clock inputs (negative and positive). 100 MHz differential.
PAD_I_REFCLKP	426	I	
PAD_O_TDN0	428	O	Transmitter differential pair (×1 lane).
PAD_O_TDP0	419	O	
PAD_O_TESTP	430	—	PCIe test pins.
PAD_O_TESTN	420	—	
PCI_PME_L	50	OD	PCI power management event output. Used to request a change in the device or system power state. The assertion and deassertion of this signal are asynchronous to the PCIe reference clock. This signal has an open-drain output structure, as per the PCI Bus Local Bus Specification, revision 2.3.
PCIE_CLKREQ_L	51	OD	PCIe clock request signal which indicates when the REFCLK to the PCIe interface can be gated. 1 = the clock can be gated. 0 = the clock is required.
PERST_L	52	I(PU)	PCIe system reset. This input is the PCIe reset as defined in the PCIe base specification version 1.1.

Table 36: BCM4375 WLCSP Signal Descriptions (Continued)

Signal Name	Bump	Type	Description
<b>WLAN GPIO Interface</b> The GPIO signals can be multiplexed via software and the JTAG_SEL pin to support other functions. See “ <a href="#">WLAN/BT GPIO Signals and Strapping Options</a> ” on page 98 and <a href="#">Table 39, GPIO Alternative Signal Functions</a> for additional details.			—
GPIO_0	108	I/O	Programmable GPIO pins.
GPIO_1	107	I/O	
GPIO_2	121	I/O	
GPIO_3	140	I/O	
GPIO_4	139	I/O	
GPIO_5	153	I/O	
GPIO_6	88	I/O	
GPIO_7	87	I/O	
GPIO_8	86	I/O	
GPIO_9	106	I/O	
GPIO_10	105	I/O	
GPIO_11	103	I/O	
GPIO_12	117	I/O	
GPIO_13	60	I/O	
GPIO_14	48	I/O	
GPIO_15	40	I/O	
GPIO_16	20	I/O	
GPIO_17	61	I/O	
GPIO_18	49	I/O	
GPIO_19	23	I/O	
GPIO_20	41	I/O	
<b>JTAG Interface</b>			
JTAG_SEL	83	I/O	JTAG select: pull high to select the JTAG interface. If the JTAG interface is not used this pin may be left floating or connected to ground. <b>NOTE:</b> See <a href="#">Table 39, GPIO Alternative Signal Functions</a> for the JTAG signal pins.

Table 36: BCM4375 WLCSP Signal Descriptions (Continued)

Signal Name	Bump	Type	Description
<b>XTAL</b>			
I_PAD_VDD_XTAL	650	I	Power supply to the XTAL.
I_PAD_XTAL_GND	645, 647, 649	I	XTAL oscillator GND.
I_PAD_XTAL_VDD_V1P12	651	I	Power supply to the XTAL.
I_PAD_XTAL_XOP	648	O	XTAL oscillator input.
O_PAD_XTAL_XON	646	I	XTAL oscillator output
<b>Clocks</b>			
BT_CLK_REQ	411	I/O	Reference clock request (shared by BT and WLAN). If not used, this can be no-connect.
LPO_IN	161	I	External sleep clock input (32.768 kHz).
<b>Bluetooth Receiver/Transceiver</b>			
O_PAD_BT_13DBMOP	628	O	Bluetooth radio output
O_PAD_BT_20DBMOP	630	O	Bluetooth radio output
O_PAD_BT_RFOP	626	I/O	Bluetooth radio shared input/output
O_PAD_BT_RFTEST	629	O	Bluetooth radio test port
<b>Bluetooth PCM</b>			
BT_PCM_CLK	387	I/O	PCM clock; can be master (output) or slave (input).
BT_PCM_IN	398	I	PCM data input.
BT_PCM_OUT	397	O	PCM data output.
BT_PCM_SYNC	384	I/O	PCM sync; can be master (output) or slave (input).
<b>Bluetooth UART</b>			
BT_UART_CTS_N	376	I	UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.
BT_UART_RTS_N	388	O	UART request-to-send. Active-low request-to-send signal for the HCI UART interface. BT LED control pin.
BT_UART_RXD	399	I	UART serial input. Serial data input for the HCI UART interface.
BT_UART_TXD	389	O	UART serial output. Serial data output for the HCI UART interface.

Table 36: BCM4375 WLCSP Signal Descriptions (Continued)

Signal Name	Bump	Type	Description
<b>Bluetooth I<sup>2</sup>S</b>			
BT_I2S_CLK	375	I/O	I <sup>2</sup> S clock, can be master (output) or slave (input).
BT_I2S_DI	401	I/O	I <sup>2</sup> S data input.
BT_I2S_DO	383	I/O	I <sup>2</sup> S data output.
BT_I2S_WS	400	I/O	I <sup>2</sup> S WS; can be master (output) or slave (input).
<b>Bluetooth GPIOs</b>			
BT_GPIO_2	410	I/O	Bluetooth general-purpose I/O.
BT_GPIO_3	362	I/O	Bluetooth general-purpose I/O.
BT_GPIO_4	412	I/O	Bluetooth general-purpose I/O.
BT_GPIO_5	413	I/O	Bluetooth general-purpose I/O.
<b>Bluetooth SLIMbus</b>			
BT_SLIMBUS_CLK	368	I/O	Bluetooth SLIMbus clock.
BT_SLIMBUS_DT	366	I/O	Bluetooth SLIMbus data.
<b>Miscellaneous</b>			
BT_AJTAG_TCK	373	I/O	Bluetooth serial I/F
BT_AJTAG_TDI	404	I/O	Bluetooth serial I/F
BT_AJTAG_TDO	403	I/O	Bluetooth serial I/F
BT_AJTAG_TMS	405	I/O	Bluetooth serial I/F
BT_DEV_WAKE	408	I/O	Bluetooth DEV_WAKE.
BT_HOST_WAKE	377	I/O	Bluetooth HOST_WAKE.
BT_REG_ON	448	I	Used by PMU to power up or power down the internal BCM4375 regulators used by the Bluetooth section. Also, when deasserted, this pin holds the Bluetooth section in reset. This pin has an internal 50 kΩ pull-down resistor that is auto-enabled and disabled when the input is low and high, respectively.
BT_TM1	406	I/O	Bluetooth test mode pin
LHL_GPIO0	132	I/O	Misc. GPIO
LHL_GPIO1	114	I/O	Misc. GPIO
LHL_GPIO2	133	I/O	Misc. GPIO I/F
LHL_GPIO3	149	I/O	Misc. GPIO

Table 36: BCM4375 WLCSP Signal Descriptions (Continued)

Signal Name	Bump	Type	Description
LHL_XTALI	190	I/O	External clock input
LHL_XTALO	189	I/O	Output
MODEHV	22	I	Connect to GND to support 1.8V RF_CW_CTRL pads. Connect to 3.3V to support 3.3V RF_SW_CTRL pads.
MODEHV1	317	I	Connect to GND to support 1.8V RF_CW_CTRL pads. Connect to 3.3V to support 3.3V RF_SW_CTRL pads.
NC	65, 66, 68, 475	I	No connect
WL_REG_ON	454	I	Used by the PMU to power up or power down the internal BCM4375 regulators used by the WLAN section. When deasserted, this pin holds the WLAN section in reset. This pin has an internal 50 kΩ pull-down resistor that is auto-enabled and disabled when the input is low and high, respectively.
<b>Bluetooth Supplies</b>			
I_PAD_BT_LDOVDD_V1P12	625	PWR	Bluetooth LDO 1.12V power supply.
I_PAD_BT_PAVDD_V3P3	638, 641	PWR	Bluetooth PA 3.3V power supply.
<b>WLAN Supplies</b>			
AFE_VDD_V1P12_AUX	573	PWR	WLAN radio 1.12V auxiliary supply.
AFE_VDD_V1P8_C0_AUX	592	PWR	WLAN radio 1.8V auxiliary core 0 supply
AFE_VDD_V1P8_C1_AUX	593	PWR	WLAN radio 1.8V auxiliary core 1 supply
AFE_VDD_V1P12_CORE0_MAIN	492	PWR	WLAN radio 1.12V main core 0 supply
AFE_VDD_V1P12_CORE1_MAIN	493	PWR	WLAN radio 1.12V main core 1 supply
PA_VDD_V3P3_CORE0_MAIN	552	PWR	WLAN radio PA 3.3V main core 0 supply
PA_VDD_V3P3_CORE1_MAIN	546	PWR	WLAN radio PA 3.3V main core 1 supply
PA2G_VDD_V3P3_C0_AUX	560, 587	PWR	WLAN radio PA 3.3V PA auxiliary core 0 supply (ePA version only)
PA2G_VDD_V3P3_C1_AUX	576, 588	PWR	WLAN radio PA 3.3V auxiliary core 1 supply (ePA version only)
PMU_TX_VDD_V1P12_CORE0_MAIN	490	PWR	WLAN radio 1.12V main core 0 supply
PMU_TX_VDD_V1P12_CORE1_MAIN	491	PWR	WLAN radio 1.12V main core 1 supply
PMU_VDD_V1P12_AUX	589	PWR	WLAN radio 1.12V supply (auxiliary slice)
PMU_VDD_V3P3_CORE0_MAIN	513	PWR	WLAN radio 3.3V core 0 supply (main slice)
PMU_VDD_V3P3_CORE1_MAIN	511	PWR	WLAN radio 3.3V core 1 supply (main slice)

Table 36: BCM4375 WLCSP Signal Descriptions (Continued)

Signal Name	Bump	Type	Description
SYNTH_VDD_V1P12_AUX	606	PWR	WLAN radio 1.12V auxiliary supply
SYNTH_VDD_V1P12_MAIN	512	PWR	WLAN radio 1.12V main supply
SYNTH_VDD_V3P3_MAIN	548	PWR	WLAN radio 3.3V main supply
TX_VDD_V1P12_C0_AUX	581, 607	PWR	WLAN radio 1.12V auxiliary core 0 supply
TX_VDD_V1P12_C1_AUX	584, 608	PWR	WLAN radio 1.12V auxiliary core 1 supply
TX_VDD_V3P3_C0_AUX	603	PWR	WLAN radio 3.3V auxiliary core 0 supply
TX_VDD_V3P3_C1_AUX	604	PWR	WLAN radio 3.3V auxiliary core 1 supply
VCO_VDD_V1P12_AUX	605	PWR	WLAN radio 1.12V supply (auxiliary slice)
VCO_VDD_V1P12_MAIN	510	PWR	WLAN radio 1.12V supply (main slice)
VCO_VDD_V3P3_MAIN	555	PWR	WLAN radio 3.3V supply (main slice)
VDD_V1P8_CORE0_MAIN	489	PWR	WLAN radio 1.8V main core 0 supply
VDD_V1P8_CORE1_MAIN	488	PWR	WLAN radio 1.8V main core 1 supply
<b>Miscellaneous Supplies</b>			
BT_VDDB	416	O	Supply monitor pin for BT
BT_VDDC	339, 381, 390, 396	PWR	1.1V core supply for BT
BT_VDDC_AAON	364	O	Supply monitor pin for BT
BT_VDDCG	367	O	Supply monitor pin for BT
BT_VDDCLDO	356, 365, 370, 372, 374	PWR	0.9V supply for BT
BT_VDDMEMLPLDO	386	PWR	0.8V retention supply for BT
BT_VDDO	379, 415	PWR	1.8V supply for BT I/O
FLL_VDDIO	72	PWR	1.8V supply for WLAN
GENERAL_VDD_V3P3_AUX	586	PWR	WLAN radio 3.3V supply
LHL_VDDO	148	PWR	1.8 supply for LHL
OTP_VDD1P8	136	PWR	OTP 1.8V supply
PAD_I_PVDD1P0	418	PWR	1.0V PCIe supply
PAD_I_RVDD1P0	422	PWR	1.0V PCIe supply
PAD_I_TVDD1P0	417	PWR	1.0V PCIe supply
VDD18_UPI	54	PWR	1.8V supply to UPI block

Table 36: BCM4375 WLCSP Signal Descriptions (Continued)

Signal Name	Bump	Type	Description
VDD_AON	31, 35, 67, 104, 115, 120, 142, 169, 173, 191, 237, 242, 248, 256, 303, 327, 333, 391	PWR	0.9V core supply for WLAN/BT
VDD_AUX	2, 15, 33, 36, 39, 53, 63, 64, 69	PWR	0.9V core supply for WLAN
VDD_DIG	102, 137, 166, 193, 224, 257, 298, 331	PWR	0.9V core supply for WLAN
VDD_MAIN	97, 112, 125, 184, 187, 231, 232, 235, 265, 293, 305, 336	PWR	0.9V core supply for WLAN
VDD_RET_WL	42, 111, 116, 253, 300, 329	PWR	0.9V core supply for WLAN
VDD_TOP	10, 19, 21, 55, 82, 90, 123, 152, 164, 170, 174, 194, 236, 258, 268, 274, 346, 351, 380	PWR	0.9V core supply for WLAN/BT
VDDIO	59, 70, 80, 85, 118	PWR	1.8V supply for WLAN I/O
VDDIO_RF	17, 37, 57, 228, 314	PWR	3.3V I/O supply for RF switch control pads
VDDP_RF	27, 29, 288, 316	PWR	1.8V supply to RF switch control pads
<b>Ground</b>			
BT_VSSC	340, 341, 342, 343, 352, 357, 358, 359, 360, 361, 363, 371, 378, 382, 385, 392, 393, 394, 395, 407, 414	GND	Core ground for Bluetooth.
I_PAD_BT_IFVSS	631, 637, 640	GND	Bluetooth IF ground.
I_PAD_BT_PAVSS	633, 634, 635, 639, 642	GND	Bluetooth PA ground.
I_PAD_BT_PLLVSS	643, 644	GND	Bluetooth PLL ground.
I_PAD_BT_RFVSS	623, 624, 627	GND	Bluetooth RF ground.

**Table 36: BCM4375 WLCSP Signal Descriptions (Continued)**

Signal Name	Bump	Type	Description
I_PAD_BT_VCOVSS	632, 636	GND	Bluetooth VCO ground.
PAD_AVDD1P0	202	PWR	Baseband PLL supply
PAD_I_PGND	429	GND	PCIe ground
PAD_I_RGND	421	GND	PCIe ground
PAD_I_TGND	427	GND	PCIe ground
PAD_AVSS	218	PWR	Baseband PLL ground
PMU_AVSS	450, 487	I	Analog ground
PVSSA	437, 439, 466, 485	I	ABUCK power stage ground
PVSSC	435, 441, 447, 461, 484	I	CBUCK power stage ground
RADIO_GND	494, 509, 514, 532, 536, 540, 544, 547, 549, 550, 551, 553, 554, 556, 559, 561, 563, 565, 572, 574, 575, 577, 580, 582, 583, 609, 622	GND	Radio ground

Table 36: BCM4375 WLCSP Signal Descriptions (Continued)

Signal Name	Bump	Type	Description
VSS	1, 3, 4, 5, 9, 11, 14, 18, 24, 26, 28, 30, 32, 34, 56, 58, 62, 71, 73, 79, 81, 84, 89, 91, 96, 98, 101, 109, 110, 113, 119, 122, 124, 126, 131, 134, 135, 138, 141, 143, 146, 150, 151, 154, 160, 165, 167, 168, 171, 172, 175, 178, 183, 185, 186, 192, 195, 201, 205, 217, 219, 223, 225, 226, 229, 230, 233, 234, 238, 239, 241, 243, 247, 249, 252, 259, 264, 266, 267, 269, 270, 271, 275, 285, 289, 290 292, 294, 297, 299, 304, 306, 313, 318, 326, 328, 330, 332, 334, 335, 337, 338, 344, 345, 353, 355, 369, 402, 409	GND	Core ground for WLAN.
VSSC	147, 162, 163, 176, 177, 188, 203, 204, 444, 486	GND	Core ground for WLAN.

Table 36: BCM4375 WLCSP Signal Descriptions (Continued)

Signal Name	Bump	Type	Description
<b>Integrated Voltage Regulators</b>			
ASR_VDDBAT5	432, 477, 478	I	Battery supply for APUCK power stage
ASR_VLX	440, 479, 480, 481, 483	O	APUCK output to inductor
CSR_VDDBAT5	433, 434, 476	I	Battery supply for CBUCK power stage
CSR_VLX	438, 443, 446, 460, 462	O	CBUCK output to inductor.
LDO_VDD0P9	436	I	Sense pin for CBUCK
LDO_VDD1P12	482	I	Input for MISCLDO and sense pin for APUCK
LDO_VDDBAT5	456, 468, 469, 470, 471, 472, 473, 474	I	Clean battery supplies for BTLDO3P3 and RFLDO3P3. Quiet supplies for CBUCK and APUCK. PMU internal always-on domain
PMU_VDDIOA	463	I	1.8V analog supply (AVDD1P8) from system platform.
PMU_VDDIOP	455	I	1.8V analog supply (AVDD1P8) from system platform.
VDDOUT_AON	465	O	Output for VMUX
VDDOUT_BT3P3	451, 452, 467	O	BTLDO3P3 output
VDDOUT_BTLDO_SNS	449	I	Sense pin for BTLDO3P3. This pin must be star-connected with VDDOUT_BT3P3 at board output cap. terminal.
VDDOUT_MEMLPLDO	464	O	MEMLPLDO output
VDDOUT_MISCLDO	442	O	MISCLDO output
VDDOUT_RF3P3	453, 457, 458, 459	O	RFLDO3P3 output for RF FEM and ePA (optional).
VDDOUT_RFLDO_SNS	431	I	RFLDO3P3 output sense. This pin must be star-connected with VOUT_RF3P3 at the board output cap. terminal.
VDDOUT_SWCORE	445	O	Power-switch output

## 10.3 WLAN/BT GPIO Signals and Strapping Options

The pins listed in [Table 37](#) and [Table 38](#) are sampled at power-on reset (POR) to determine the various operating modes. Sampling occurs a few milliseconds after an internal POR or deassertion of the external POR. After the POR, each pin assumes the GPIO or alternative function specified in the signal descriptions table. Each strapping option pin has an internal pull-up (PU) or pull-down (PD) resistor that determines the default mode. To change the mode, connect an external PU resistor to VDDIO or a PD resistor to GND, using a 10 kΩ resistor or less.

**NOTE:** Refer to the reference board schematics for more information.

**Table 37: BT GPIO Functions and Strapping Options**

Pin Name	Default Function	Description
BT_GPIO2	0	1: BT Serial Flash is present. 0: BT Serial Flash is absent (default).

**NOTE:** Not valid on wireless charging platform.

[Table 38](#) provides the BCM4375 GPIO strapping options.

**Table 38: BCM4375 GPIO Strapping Options**

Pin Name	Default Pull During Strapping	Description
GPIO_7	0	Debug access port select (DAP SEL) 0: Not selected 1: Selected
GPIO_17	0	OTP select 0: OTP 1: Reserved
GPIO_20	1	Reserved
GPIO_14	0	Bluetooth over UART select 0: Reserved 1: BT over UART
GPIO_16	1	Internal PA (iPA) gain select
MODEHV/MODEHV1	0	VDDIO_RF voltage select 0: 1.8V support on RF_SW_CTRL pads 1: 3.3V support on RF_SW_CTRL pads

## 10.4 GPIO Alternative Signal Functions

Table 39: GPIO Alternative Signal Functions

Pin	Function Name and Number															
	Power-On Default	Pin Name	GPIO-0	FAST_UART/ GPIO_1	GCI-0	GCI-1	DBG_UART	SPI/I2C	Reserved	MISC-0	MISC-1	MISC-2	IND	PDN	PUP	TRI
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
GPIO_0	TRISTATE_IND	WL_HOST_WAKE/ GPIO_0	GPIO_8	—	GCI_GPIO_0	GCI_GPIO_11	—	—	—	—	—	—	—	—	—	—
GPIO_1	TRISTATE_IND	WL_DEV_WAKE/ GPIO_1	GPIO_9	—	GCI_GPIO_1	GCI_GPIO_12	—	—	—	RF_DISABLE_L	—	—	—	—	—	—
GPIO_2	JTAG_SEL? TCK: TRISTATE_IND	GPIO_2	GPIO_10	FAST_UART_RX	GCI_GPIO_2	GCI_GPIO_13	UART_DBG_RX	—	—	TCK	MUXED_RF_SW_CTRL0	—	—	—	—	—
GPIO_3	JTAG_SEL? TMS: TRISTATE_IND	GPIO_3	GPIO_11	FAST_UART_TX	GCI_GPIO_3	GCI_GPIO_14	UART_DBG_TX	—	—	TMS	MUXED_RF_SW_CTRL1	—	—	—	—	—
GPIO_4	JTAG_SEL? TDI: TRISTATE_IND	GPIO_4	GPIO_12	FAST_UART_CTS_IN	GCI_GPIO_4	GCI_GPIO_15	—	—	—	TDI	MUXED_RF_SW_CTRL2	—	—	—	—	—
GPIO_5	JTAG_SEL? TDO: TRISTATE_IND	GPIO_5	GPIO_13	FAST_UART_RTS_OUT	GCI_GPIO_0	GCI_GPIO_5	—	—	—	TDO	MUXED_RF_SW_CTRL3	—	—	—	—	—
GPIO_6	JTAG_SEL? TRST_L: TRISTATE_IND	GPIO_6	GPIO_14	—	GCI_GPIO_1	GCI_GPIO_6	UART_DBG_RX	—	—	TRST_L	MUXED_RF_SW_CTRL4	—	—	—	—	—
GPIO_7	TRISTATE_IND	GPIO_7	GPIO_15	—	GCI_GPIO_2	GCI_GPIO_7	UART_DBG_TX	—	—	PMU_TEST_O	SWD/JTAG SELECT.	—	—	—	—	—
GPIO_8	TRISTATE_IND	GPIO_8	GPIO_0	FAST_UART_RX	GCI_GPIO_3	GCI_GPIO_8	—	GSIO_SDI	—	—	—	—	—	—	—	—
GPIO_9	TRISTATE_IND	GPIO_9	GPIO_1	FAST_UART_TX	GCI_GPIO_4	GCI_GPIO_9	—	GSIO_SDO	—	—	—	—	—	—	—	—
GPIO_10	TRISTATE_IND	GPIO_10	GPIO_2	FAST_UART_CTS_IN	GCI_GPIO_0	GCI_GPIO_10	UART_DBG_RX	GSIO_CSN	—	—	—	—	—	—	—	—
GPIO_11	TRISTATE_IND	GPIO_11	GPIO_3	FAST_UART_RTS_OUT	GCI_GPIO_1	GCI_GPIO_11	UART_DBG_TX	GSIO_CLK	—	—	—	—	—	—	—	—

Table 39: GPIO Alternative Signal Functions (Continued)

Pin	Function Name and Number															
	Power-On Default	Pin Name	GPIO-0	FAST UART/ GPIO 1	GCI-0	GCI-1	DBG UART	SPI/I2C	Reserved	MISC-0	MISC-1	MISC-2	IND	PDN	PUP	TRI
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
GPIO_12	TRISTATE_IND	WL_LED1/ GPIO_12	GPIO_4	—	GCI_GPIO_2	GCI_GPIO_12	UART_DBG_RX	—	—	—	—	—	—	—	—	—
GPIO_13	TRISTATE_IND	WL_LED0/ GPIO_13	GPIO_5	—	GCI_GPIO_3	GCI_GPIO_13	UART_DBG_TX	SDIO_CLK	Reserved	—	—	—	—	—	—	—
GPIO_14	TRISTATE_IND	GPIO_14	GPIO_6	—	GCI_GPIO_4	GCI_GPIO_14	—	—	—	—	—	—	—	—	—	—
GPIO_15	TRISTATE_IND	GPIO_15	GPIO_7	—	—	GCI_GPIO_15	—	SDIO_CMD	Reserved	—	—	—	—	—	—	—
GPIO_16	TRISTATE_IND	GPIO_16	GPIO_11	—	GCI_GPIO_0	—	—	SDIO_D0	—	—	—	—	—	—	—	—
GPIO_17	TRISTATE_IND	GPIO_17	GPIO_12	—	GCI_GPIO_1	—	—	SDIO_D1	—	—	—	—	—	—	—	—
GPIO_18	TRISTATE_IND	GPIO_18	GPIO_13	—	GCI_GPIO_2	—	—	SDIO_D2	Reserved	—	—	—	—	—	—	—
GPIO_19	TRISTATE_IND	GPIO_19	GPIO_14	—	GCI_GPIO_3	—	—	SDIO_D3	Reserved	—	—	—	—	—	—	—
GPIO_20	TRISTATE_IND	GPIO_20	GPIO_15	—	GCI_GPIO_4	—	—	—	—	—	—	—	—	—	—	—
RF_SW_CTRL_0	RF_SW_CTRL_0	RF_SW_CTRL_0	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RF_SW_CTRL_1	RF_SW_CTRL_1	RF_SW_CTRL_1	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RF_SW_CTRL_2	RF_SW_CTRL_2	RF_SW_CTRL_2	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RF_SW_CTRL_3	RF_SW_CTRL_3	RF_SW_CTRL_3	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RF_SW_CTRL_4	RF_SW_CTRL_4	RF_SW_CTRL_4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RF_SW_CTRL_5	RF_SW_CTRL_5	RF_SW_CTRL_5	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RF_SW_CTRL_6	RF_SW_CTRL_6	RF_SW_CTRL_6	GPIO_8	GPIO_0	—	GCI_GPIO_8	—	GSIO_SDI	—	—	—	—	—	—	—	—
RF_SW_CTRL_7	RF_SW_CTRL_7	RF_SW_CTRL_7	GPIO_9	GPIO_1	—	GCI_GPIO_9	—	GSIO_SDO	—	—	—	—	—	—	—	—
RF_SW_CTRL_8	RF_SW_CTRL_8	RF_SW_CTRL_8	GPIO_10	GPIO_2	—	GCI_GPIO_10	UART_DBG_RX	GSIO_CSN	—	—	—	—	—	—	—	—
RF_SW_CTRL_9	RF_SW_CTRL_9	RF_SW_CTRL_9	GPIO_11	GPIO_3	—	GCI_GPIO_11	UART_DBG_TX	GSIO_CLK	—	PALDO_PU	—	—	—	—	—	—
RF_SW_CTRL_10	RF_SW_CTRL_10	RF_SW_CTRL_10	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Table 39: GPIO Alternative Signal Functions (Continued)

Pin	Function Name and Number															
	Power-On Default	Pin Name	GPIO-0	FAST UART/ GPIO 1	GCI-0	GCI-1	DBG UART	SPI/I2C	Reserved	MISC-0	MISC-1	MISC-2	IND	PDN	PUP	TRI
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
RF_SW_CTRL_11	RF_SW_CTRL_11	RF_SW_CTRL_11	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RF_SW_CTRL_12	RF_SW_CTRL_12	RF_SW_CTRL_12	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RF_SW_CTRL_13	RF_SW_CTRL_13	RF_SW_CTRL_13	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RF_SW_CTRL_14	RF_SW_CTRL_14	RF_SW_CTRL_14	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RF_SW_CTRL_15	RF_SW_CTRL_15	RF_SW_CTRL_15	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RF_SW_CTRL_16	RF_SW_CTRL_16	RF_SW_CTRL_16	GPIO_12	GPIO_4	—	GCI_GPIO_12	—	GSIO_CLK	—	—	—	—	—	—	—	—
RF_SW_CTRL_17	RF_SW_CTRL_17	RF_SW_CTRL_17	GPIO_13	GPIO_5	—	GCI_GPIO_13	—	GSIO_CSN	—	—	—	—	—	—	—	—
RF_SW_CTRL_18	RF_SW_CTRL_18	RF_SW_CTRL_18	GPIO_14	GPIO_6	—	GCI_GPIO_14	UART_DBG_TX	GSIO_SDO	—	—	—	—	—	—	—	—
RF_SW_CTRL_19	RF_SW_CTRL_19	RF_SW_CTRL_19	GPIO_15	GPIO_7	—	GCI_GPIO_15	UART_DBG_RX	GSIO_SDI	—	PALDO_PD	—	—	—	—	—	—
RF_SW_CTRL_20	RF_SW_CTRL_20	RF_SW_CTRL_20	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RF_SW_CTRL_21	RF_SW_CTRL_21	RF_SW_CTRL_21	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RF_SW_CTRL_22	RF_SW_CTRL_22	RF_SW_CTRL_22	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RF_SW_CTRL_23	RF_SW_CTRL_23	RF_SW_CTRL_23	RFFE_SCLK	—	—	—	—	—	—	—	—	—	—	—	—	—
RF_SW_CTRL_24	RF_SW_CTRL_24	RF_SW_CTRL_24	RFFE_SDATA	—	—	—	—	—	—	—	—	—	—	—	—	—

Table 40 defines the status for all BCM4375 GPIOs based on the tristate test mode.

Table 40: GPIO Status Versus Test Modes

Test Mode	Function Select
TRISTATE_IND	12
TRISTATE_PDN	13
TRISTATE_PUP	14
TRISTATE	15

## 10.5 I/O States

The following notations are used in [Table 41](#):

- I: Input signal
- O: Output signal
- I/O: Input/Output signal
- PU = Pulled up
- PD = Pulled down
- NoPull = Neither pulled up nor pulled down
- Where applicable, the default value is shown in brackets (for example, [default value])

**Table 41: WLAN-Side of PMIO States**

<i>Name</i>	<i>I/O</i>	<i>Keeper</i>	<i>Active Mode</i>	<i>Low-Power State/Sleep (All Power Present)</i>	<i>Power-down (BT_REG_ON and WL_REG_ON Held Low)</i>	<i>Out-of-Reset; Before SW Download (BT_REG_ON High; WL_REG_ON High)</i>	<i>(WL_REG_ON High and BT_REG_ON = 0) and VDDIOs are Present</i>	<i>Power Rail</i>
WL_REG_ON BT_REG_ON	I	N	I: PD Pull-down auto disabled	I: PD Pull-down auto disabled	I: PD (of 50K)	I: PD (of 50K)	I: PD (of 50K)	—
GPIO_0	I/O	Y	I/O: PU, PD, NoPull Programmable [PD]	I/O: PU, PD, NoPull Programmable [PD]	High-Z, NoPull	I: PD	I: PD	VDDIO
GPIO_1	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_2	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull <sup>a</sup>	I: NoPull	VDDIO
GPIO_3	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull <sup>a</sup>	I: NoPull	VDDIO
GPIO_4	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull <sup>a</sup>	I: NoPull	VDDIO
GPIO_5	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull <sup>a</sup>	I: NoPull	VDDIO
GPIO_6	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull <sup>a</sup>	I: NoPull	VDDIO
GPIO_7	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_8	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_9	I/O	Y	I/O: PU, PD, NoPull Programmable [PU]	I/O: PU, PD, NoPull Programmable [PU]	I: PU	I: NoPull	I: NoPull	VDDIO

Table 41: WLAN-Side of PMIO States (Continued)

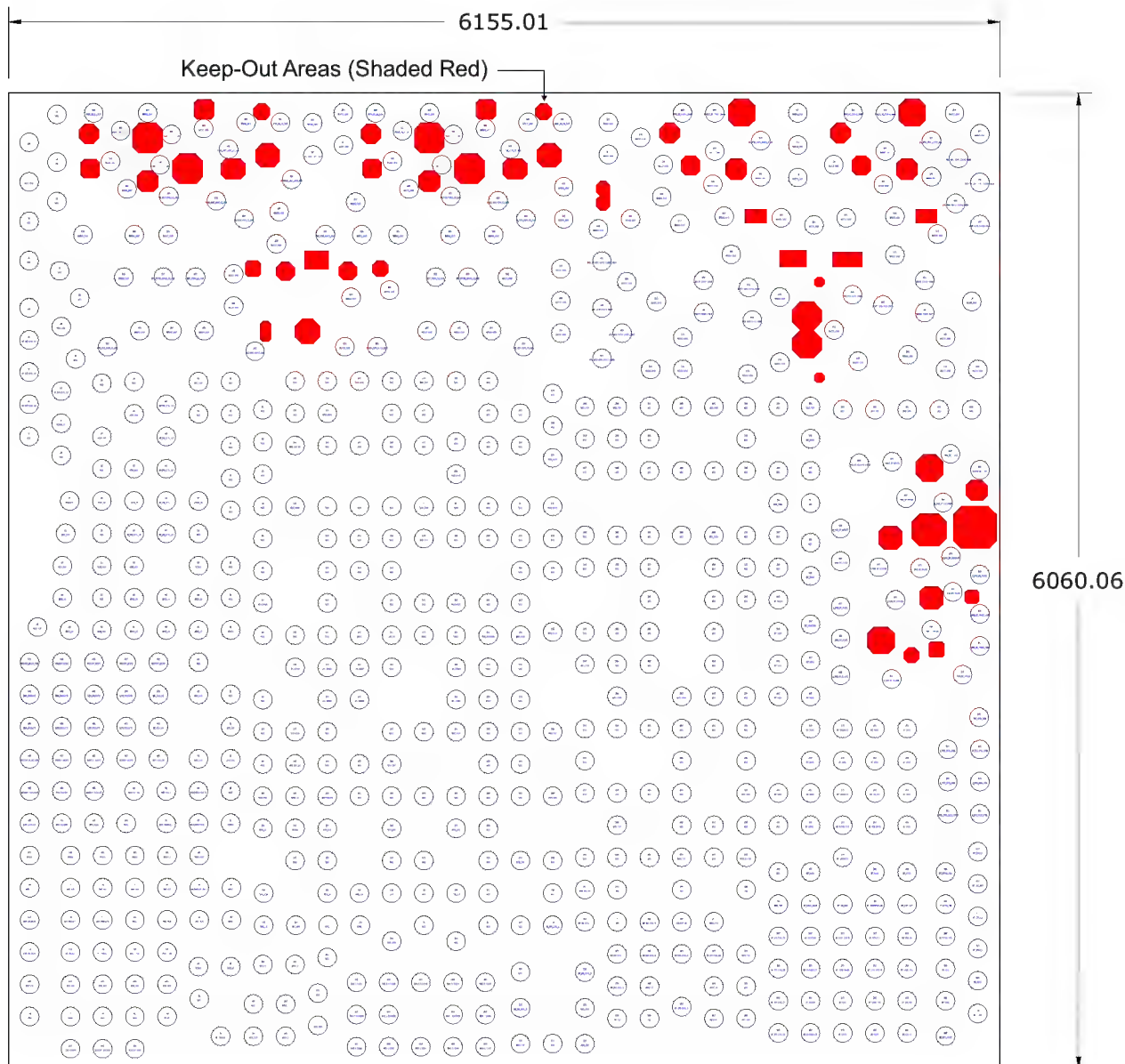
Name	I/O	Keeper	Active Mode	Low-Power State/Sleep (All Power Present)	Power-down (BT_REG_ON and WL_REG_ON Held Low)	Out-of-Reset; Before SW Download (BT_REG_ON High; WL_REG_ON High)	(WL_REG_ON High and BT_REG_ON = 0) and VDDIOs are Present	Power Rail
GPIO_10	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_11	I/O	Y	I/O: PU, PD, NoPull Programmable [PU]	I/O: PU, PD, NoPull Programmable [PU]	I: PU	I: NoPull	I: NoPull	VDDIO
GPIO_12	I/O	N	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_13	I/O	N	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_14	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_15	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_16	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_17	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_18	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_19	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
RF_SW_CTRL_X	O	N	O: NoPull	O: NoPull	High-Z, NoPull	O: NoPull	O: NoPull	VDDIO_RF

a. When JTAG is not enabled on the GPIO.

## 10.6 Ball Map and Keep-Out Areas

Figure 24 shows the BCM4375 WLCSP PCB layout keep-out areas.

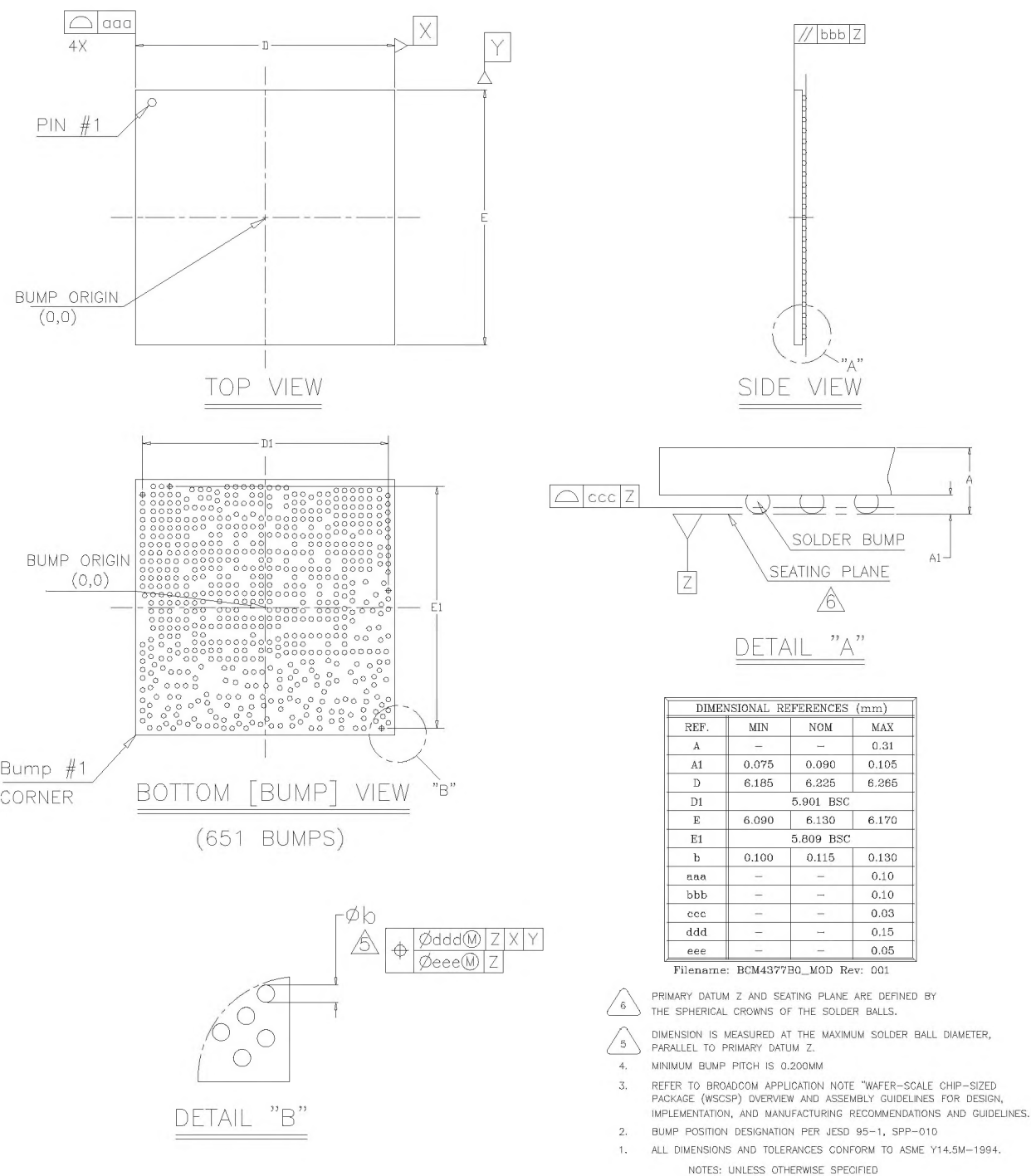
**Figure 24: BCM4375 WLCSP PCB Layout Keep-Out Areas (Package Top View, Bumps Facing Down)**



10.7 Mechanical Drawing

Figure 25 is the mechanical drawing for the BCM4375.

Figure 25: BCM4375 WLCSP Mechanical Drawing



## Chapter 11: Ordering Information

**Table 42: Ordering Information**

Part Number	Package	Description	Ambient Operating Temperature
<b>Pre-Production Ordering</b>			
BCM4375B1XKWBG-TE	B1 Revision, 651-bump WLCSP (6.225 mm × 6.130 mm, 0.2 mm pitch)	Dual-band 2.4 GHz and 5 GHz WLAN, and Bluetooth (TSMC Fab., ASE Assembly)	–30°C to 85°C
BCM4375B1XKWBG-TN	B1 Revision, 651-bump WLCSP (6.225 mm × 6.130 mm, 0.2 mm pitch)	Dual-band 2.4 GHz and 5 GHz WLAN, and Bluetooth (TSMC Fab., SPIL Assembly)	–30°C to 85°C
BCM4375B4XKFFBG	B1 Revision, 394-ball FCFBGA (10 mm × 10 mm, 0.40 mm pitch)	Dual-band 2.4 GHz and 5 GHz WLAN, and Bluetooth (TSMC Fab., SPIL Assembly)	–30°C to 85°C
BCM4375B0XKWBG-TE	B0 Revision, 651-bump WLCSP (6.225 mm × 6.130 mm, 0.2 mm pitch)	Dual-band 2.4 GHz and 5 GHz WLAN, and Bluetooth (TSMC Fab., ASE Assembly)	–30°C to 85°C
<b>Production Ordering</b>			
BCM4375B1XKWBG	B1 Revision, 651-bump WLCSP (6.225 mm × 6.130 mm, 0.2 mm pitch)	Dual-band 2.4 GHz and 5 GHz WLAN, and Bluetooth	–30°C to 85°C

## Revision History

### 4375-DS104; August 14, 2018

- Updated [Table 42, Ordering Information](#).

### 4375-DS103; July 6, 2018

- Updated Table 25, Bluetooth Transmitter RF Specifications.
- Updated Table 28, WLAN 2.4 GHz Receiver Performance Specifications.
- Updated Table 29, WLAN 2.4 GHz Transmitter Performance Specifications.
- Updated Table 30, WLAN 5 GHz Receiver Performance Specifications.
- Updated Table 31, WLAN 5 GHz Transmitter Performance Specifications.
- Updated Table 33, Typical WLAN Power Consumption.
- Updated Table 34, Bluetooth and BLE Current Consumption.

### 4375-DS102; April 27, 2018

- Updated Electrostatic Discharge Specifications.

### 4375-DS101; April 17, 2018

- Updated Figure 1, BCM4375 Functional Block Diagram.
- Updated the Features on page 2.
- Updated Table 3, Recommended Operating Conditions and DC Characteristics.
- Updated Power Supplies and Power Management.
- Updated Crystal Interface and Clock Generation.
- Updated Figure 21, Port Locations for Bluetooth Testing.
- Updated Table 25, Bluetooth Transmitter RF Specifications.
- Updated Figure 22, Port Locations for WLAN Testing.
- Updated Table 28, WLAN 2.4 GHz Receiver Performance Specifications.
- Updated Table 29, WLAN 2.4 GHz Transmitter Performance Specifications.
- Updated Table 30, WLAN 5 GHz Receiver Performance Specifications.
- Updated Table 31, WLAN 5 GHz Transmitter Performance Specifications.
- Updated Table 33, Typical WLAN Power Consumption.
- Updated Table 34, Bluetooth and BLE Current Consumption.
- Updated Table 36, BCM4375 WLCSP Signal Descriptions.
- Updated Table 42, Ordering Information.

### 4375-DS100; July 13, 2017

Initial release.

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